SYMPOSIUM H

Giant-Area Electronics on Nonconventional Substrates

March 31 - April 1, 2005

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* Invited paper

SESSION H1: Film Growth and Processing for Giant Area Electronics
Chair: Martin Stutzmann
Thursday Morning, March 31, 2005
Room 2008 (Moscone West)

9:00 AM *H1.1
Large-area Deposition of Amorphous Silicon Alloys Using a Roll-to-roll Operation. Subhendu Guha, Ovonic, United Solar Systems Corporation, Auburn Hills, Michigan.

Many modern electronic devices need to be lightweight and flexible to meet diversified customer demands. At United Solar, we have been manufacturing amorphous silicon alloy solar cells on flexible stainless steel substrates. Rolls of stainless steel, one and a half -mile long, 14 inches wide and 5 mil thick go through the following processors to complete the solar cell structure: 1. wash machine that washes the roll, 2. back-reflector machine that sputters a bi-layer of Al and ZnO, 3. a-Si alloy processor that deposits nine layers of amorphous silicon and amorphous silicon germanium alloys by plasma-assisted chemical vapor deposition, and 4. an anti-reflection coating machine that sputters a layer of Indium Tin Oxide. The 1.5-mile long solar cell is next cut and processed to make a variety of photovoltaic products. We have also used 1 mil thick polyimide to deposit solar cells using the roll-to-roll processor. The cell performance is similar to that on stainless steel; specific power exceeding 1000 W/kg has been achieved.

9:30 AM H1.2
Gas Permeation Barrier Films Grown by Atomic Layer Deposition on Polyester and Polyimide Substrates. Robert Scott McLean[1], Peter F. Carcia[1], Markus Groner[2], Steven George[2], Yoshi Senzaki[3] and Seung Park[3]; [1]CR&D, Dupont Co., Wilmington, Delaware; [2]Dept. of Chemistry and Biochemistry, University of Colorado, Boulder, Colorado; [3]Aviza Technology, Scotts Valley, California.

Increasingly, prospective electronic and display devices on inexpensive flexible substrates are comprised of organic materials. While their low processing temperature is compatible with these substrates and the electronic performance satisfactory, the environmental stability is often not, because of reactivity with air and moisture. The problem is further exacerbated by facile permeation of atmospheric gases through flexible plastic substrates. To be useable in electronic and display devices, plastic substrates will require barrier coatings that exclude atmospheric gases. Estimates are that these barrier coatings need to reduce the permeability of a bare plastic substrate by a factor of 10E4 to 10E6. In this presentation we show that thin inorganic coatings produced by atomic layer deposition (ALD) offer the prospect of a simple ultra-barrier technology for plastic substrates for use in flexible electronics. Specifically, we describe the barrier properties of very thin (< 25 nm) Al2O3 and HfO2 films grown by ALD on polyethylene terephthalate (PET), polyethylene naphthalate (PEN) and Kapton* polyimide films. The substrate growth temperature was between 100 C and 200 C. These films were amorphous with featureless microstructure. Reduction in O2/H2O permeation through ALD Al2O3, grown directly on plastic substrates, was excellent, at least 10,000 X better than the bare substrate. However, equivalent performance with ALD HfO2 required the plastic substrates to be pre-coated with a thin seed layer of either e-beam evaporated Al2O3 or SiO2. Within the limited thickness range (10nm-25 nm), we investigated, barrier properties improved with ALD film thickness and growth temperature.

9:45 AM H1.3
High-K Polymerized Dichlorotetramethyldisiloxane Films Deposited by Radio Frequency Pulsed Plasma for Gate Dielectrics in Flexible Polymer FETs. Yifan Xu[1], Paul R. Berger[1,2], Jai Cho[3] and Richard B. Timmons[3]; [1]Electrical and Computer Engineering, The Ohio State University, Columbus, Ohio; [2]Physics, The Ohio State University, Columbus, Ohio; [3]Chemistry and Biochemistry, University of Texas at Arlington, Arlington, Texas.

Polymerized dichlorotetramethyldisiloxane (DCTMDS) films deposited by radio frequency pulsed plasma polymerization (PPP) demonstrated very high dielectric constants for an organic-based system, in the range of 7 to 10, and enable all-polymer flexible electronics. High-k gate dielectrics are highly desirable for metal-insulator-semiconductor field effect transistors (MISFET) as the capacitance of the gate insulator scales with permittivity, which is in turn proportional to the FET output current. The PPP process readily lends itself to deposition of thin gate dielectric films above or below electroactive polymer channels with little to no observable layer intermixing. The PPP DCTMDS dielectric constants were determined from C-V measurements of Au/DCTMDS/Si MIS structures at 1 MHz. The magnitude of the dielectric constant depends on polarizability of the polymer and its molar volume given by the Clausius-Mossotti equation. The high dielectric constants of PPP DCTMDS films is due to the high polarizability of the -Cl group. The few reports of flexible polymer dielectric films used as gate insulators in polymer FETs (PFET) utilized polyvinylphenol or polyimide, which generally have dielectric constants ranging from 3 to 3.5, compared to the more common choice for PFETs of rigid SiO_2 which has a dielectric constant of 3.9. The design of experiments for this PPP DCTMDS dielectric film study explored two variables. Part one examined how duty cycle affects the permittivity of polymerized DCTMDS dielectric films. Part two identified the optimal temperature window for post-deposition annealing to reduce the leakage current. The pulsed plasma duty cycle (ON/OFF) resulted in higher dielectric constant DCTMDS films for higher duty cycles. The variation of dielectric constants does not show any trend with varying film thicknesses, indicating that the thickness of the deposited films is not significant for controlling permittivity. Post-deposition annealing improves the electrical integrity of PPP DCTMDS films. The leakage current of the PPP DCTMDS reduces with higher annealing temperature up to 200 ^oC, but heating above 200 ^oC elevates the leakage current, due probably to the volatizing low molecular weight oligomers or breakage of relatively weak chemical bonds. Therefore, the optimal annealing temperature was in the range of 150 ^oC to 200 ^oC. Film shrinkage in this temperature window was minimal and within the measurement uncertainty. Annealed samples have low leakage current densities below 0.1 pA/ μm^2 at 10 V for film thicknesses about 100 nm. The PPP DCTMDS films are resistant to typical chemical solvents, and have withstood conventional photolithographic processing with no observable film shrinkage, warping or peeling. Film adhesion was excellent and withstood the scotch tape test. The high performance of polymerized DCTMDS films (high dielectric constant and low leakage current density) makes it a promising insulator for flexible polymer circuits.

10:30 AM H1.4
High Performance, Low Voltage Organic Thin-Film Transistors and Circuits. Stijn De Vusser[1,2], Soeren Steudel[1,2], Kris Myny[1], Jan Genoe[1] and Paul Heremans[1,2]; [1]MCP, IMEC, Heverlee, Belgium; [2]ESAT, KULeuven, Heverlee, Belgium.

Organic Thin-Film Transistors (OTFT's) have gained increasing interest since the last decade, as they are a promising technology for low-cost electronic circuits. Potential applications include driving devices for active matrix organic displays, large area electronic circuits and RF-ID tags. Evaporated pentacene is one of the most frequently used organic semiconductors, with a performance comparable to amorphous Si. Here, we report on high performance, low voltage pentacene OTFT's and circuits. Devices and circuits were fabricated on a glass wafer. Ti was used as the gate layer, SiO_2 as the gate dielectric, and Au as source and drain electrodes, respectively. The pentacene was deposited on top of the Au electrodes. Inverters and ring oscillators have been designed and fabricated. At 15V supply voltage, we have observed invertors showing a voltage gain of 9 and an output swing of 13V. The ring oscillators consist of a chain of 5 inverters, followed by two buffer stages. The output of the last inverter in the chain was fed back to serve as the input of the first inverter. Oscillations started at supply voltages as low as 8.5V. At a supply voltage of only 15V, a stage delay time of 1μs is calculated. This value is considered to be very fast, as compared to literature values. The output buffer speed limits the output swing in the current design, but still a figure beyond 8V is obtained at 15V supply voltage. In contrast to previously published results, our oscillators operate at high speed, even at low supply voltages. Comparably fast ring oscillators have been reported before; however, these required typical supply voltages of more than 70V for a comparable delay time [Appl. Phys. Lett. 81, 1735 (2002)]. The low-voltage aspect of our work is crucial, as this power voltage can be obtained from rectification using an organic (pentacene) diode. These results have an important impact on the realization of RF-ID tags: by integrating our circuits with an organic diode, the fabrication of organic RF-ID tags comes closer. In conclusion, we have fabricated ring oscillators based on OTFT's. Compared to previously published results, our circuits perform comparably well or better; however, the supply voltage our circuits require for this performance is substantially lower than what has been published before. This is an important step towards the realization of organic RF-ID tags.

10:45 AM H1.5
Selective Nucleation and Growth of Large Grain Polycrystalline GaAs. Cary Glenn Allen[1], J. D. Beach[1], A. A. Khandekar[2], J. D. Dorr[1], R. T. Collins[1], T. F. Kuech[2], R. Caputo[1], R. E. Hollingsworth[3], C. K. Inoki[4] and T. S. Kuan[4]; [1]Physics, Colorado School of Mines, Golden, Colorado; [2]Chemical Engineering, University of Wisconsin, Madison, Wisconsin; [3]ITN Energy Systems Inc., Littleton, Colorado; [4]Physics, SUNY at Albany, Albany, New York.

We are investigating the growth of polycrystalline GaAs with controlled grain size for use as a polycrystalline thin film photovoltaic material. GaAs and its alloys have produced extremely efficient single crystal photovoltaic cells, but their performance in polycrystalline form has been poor due to minority carrier recombination at defects in the film and, in particular, at grain boundaries. Typical thin-film deposition techniques for polycrystalline GaAs tend to proceed with an uncontrolled nucleation step followed by growth. This leads to small, randomly oriented grains and high densities of grain boundaries. This talk presents a method for controlled nucleation followed by selective gallium deposition on the nucleation sites which has the potential to produce large grain films on a broad range of thin film PV substrates. While the above processes have been developed for thin film photovoltaics, they also have application to precisely positioning semiconductor dots on interesting substrates. Initial work focused on process development using Si substrates. Submicron diameter gallium deposits are fabricated on Si using a combination of near-field scanning optical microscopy (NSOM) based lithography and gallium electrodeposition. A silicon substrate is coated with a thin layer of photoresist, and the NSOM is used to expose an array of holes in it. After the holes are developed, gallium is electrodeposited into the holes from an aqueous GaCl3 solution. In the next step, an arsine anneal in a chemical vapor deposition reactor converts the nucleated gallium to GaAs. Subsequent metalorganic chemical vapor deposition (MOCVD) growth occurs selectively on these dots, enlarging them and forming regular arrays of GaAs disks up to 20 microns in diameter. Transmission electron microscopy, AFM, NSOM, and photoluminescence have been used to document steps in the process and indicate reasonable material quality. This work validates the fundamental concept of controlling polycrystalline GaAs grain size by controlling the nucleation step, but is not practical for low cost devices. Results from alternative approaches to controlled nucleation in large area films will be presented including microcontact printing of Ga containing solutions directly on the substrate and direct decomposition of triethyl gallium in the MOCVD reactor. We will also discuss extensions of this approach to alternative substrates, and possible methods for defining the orientation of the GaAs seed crystallites.

11:00 AM H1.6
Incorporating Optical Fiber Based Sensors into Fabrics.
Anuj Dhawan[2], Tushar Ghosh[2] and John Muth[1]; [1]ECE Dept Box 7911, NC State University, Raleigh, North Carolina; [2]College of Textiles, NC State University, Raleigh, North Carolina.

Optical fiber sensors can be sensitive, environmentally robust, immune to electromagnetic interference and remotely interrogated. By incorporating optical fibers into woven and non-woven fabrics these sensors can be distributed across large areas. Recent work addressing the challenges of incorporating optical fibers into woven and non-woven fabrics will be addressed. In the weaving processes, macroscopic, and microscopic bending is an issue due to the fibers going over and under the yarns. Bending losses are quantified by placing the optical fabric on frames of different radii of curvature and measuring the resulting loss of transmitted light. As an example non-woven process, electrospinning was used to overlay a net of sub-micron diameter fibers over the optical fiber. This holds the optical fiber in place while still permitting flexibility. To form sensors, standard telecommunications grade optical fiber was modified by tapering the fibers such that the evanescent wave extended into the environment. The tapered portions of the fibers were then coated with environmentally sensitive thin films deposited by pulsed laser deposition and incorporated into the fabrics. The use of a pulsed deposition method permitted a variety of coating to be tested including metallic nanoparticles with strong plasmon resonances that were sensitive to variations in the surrounding index of refraction.

11:15 AM H1.7
Low-Damage Patterning Technique of Pentacene using a SiN_x/PVA-Photoresist Multi-Layer Mask.
Nobukazu Hirai, Nobuhide Yoneya, Noriyuki Kawashima, Makoto Noda, Kazumasa Nomoto, Masaru Wada and Jiro Kasahara; Fusion Domain Laboratory, Materials Laboratories, Sony Corporation, Tokyo, Japan.

We discuss a degradation mechanism for patterning process of pentacene using PVA photoresist and present a low-damage pattering technique. The low-damage patterning technique of an active layer of OTFT is indispensable for device integration. The patterning process for organic semiconductors is problematic because of their poor resistance to organic solvents. Therefore, shadow mask techniques are often used, but cannot be applied to fine patterning. T. N. Jackson *etal.* performed fine patterning of a pentacene layer using an O_2-plasma with a mask of water-soluble poly (vinyl alcohol) (PVA) with a hexavalent chromium (Cr(VI)) crosslinking agent [1]. However, Cr(VI) is not a preferable material because of its hazardous nature. We performed structural and electrical investigations on the degradation mode of pentacene TFT in patterning process using PVA photoresist. XRD analysis revealed that PVA photoresist and its solvent of water didn't affect the crystallinity of pentacene, although a typical photoresist solvent, such as PGMEA, induced a structural-phase transition from thin-film phase to bulk phase. Reflecting on this fact, on-current of pentacene TFT was hardly affected by the PVA photoresist as opposed to the PGMEA. However, a considerable increase in off-current was observed even in the case of the PVA photoresist. The off-current increase was investigated for two types of PVA; one with a photosensitive functional group and the other without it. We observed an off-current increase only in the case of PVA photoresist with the photosensitive functional group. Therefore, off-current must be caused by an interaction between the photosensitive functional group of PVA photoresist and pentacene. In fact, off-current could be suppressed by the insertion of a SiN_x layer between the pentacene and the PVA photoresist layers. An O_2-plasma etching of a pentacene layer also increased off-current. We found that the off-current could only be decreased by annealing the TFT in a vacuum. This phenomenon indicated that oxygen doping caused by the O_2-plasma etching of a pentacene layer could be de-doped by thermal annealing in a vacuum. Based on these results, we developed a low-damage patterning technique using O_2-plasma etching with a mask of a SiN_x/PVA-photoresist multi-layer mask followed by annealing in a vacuum. This technique was used to demonstrate a 2.5-inch 160x120 pixel pentacene-TFT addressing AM-TN-LCD. [1] T. N. Jackson *etal.*, 42nd Electronic Materials Conference Digest, p.24, 2000.

11:30 AM H1.8
Direct Patterning of Organic Materials and Metals Using a Micromachined Printhead.
J. Chen[1], V. Leblanc[1], S. H. Kang[1], M. A. Baldo[1], P. J. Benning[2], V. Bulović[1] and M. A. Schmidt[1]; [1]Microelectronics Technology Laboratory, Massachusetts Institute of Technology, Cambridge, Massachusetts; [2]Hewlett-Packard Company, Corvallis, Oregon.

We report that an electrostatically actuated micromachined (MEMS) shutter integrated with an x-y-z manipulator was successfully used to modulate the flux of evaporated organic semiconductors and metals, and generate patterns of the deposited materials. This printing scheme could enable patterning of large area organic optoelectronic devices on diverse substrates. The micromachined printhead reported here consists of a free-standing silicon microshutter actuated over a 25 microns square aperture by a comb-drive actuator. The device is fabricated starting with a SOI wafer and using Deep Reactive Ion Etching to pattern both the through-wafer aperture and the free-standing structure and actuation mechanism. An operating voltage of 30 V is needed to obstruct the aperture with the microshutter. The simulated first mechanical resonant frequency of the device is 6 kHz. We tested the printing method in a vacuum chamber by depositing organic semiconductor, Alq3, and silver on glass substrates. An effusion cell was used to sublime the active materials, with its height adjustable to facilitate study of the effects of distance between the source and the microshutter. The microshutter was mounted on a ceramic package with electrical feedthrough at a fixed position in the chamber. The substrate on which material is deposited was attached to a programmable x-y-z manipulator with stepping motors to allow relative motion of the substrate with respect to the microshutter for arbitrary pattern printing. 30x30 micron pixel size Alq3 (tris(8-hydroxyqunolinato) aluminum) matrix was directly printed on ITO coated glass substrate. The influence of deposition conditions on the pixel profile was studied with atomic force microscopy and light interference microscopy (WYKO). The results show that the molecular jet print technique is capable of patterning small molecule organic light emitting devices at high resolution. 30 micron wide metal patterns directly written at 1100 °C using the same technique was also demonstrated.

11:45 AM H1.9
Highly Efficient Flexible Devices using a Statistical Copolymer of Oxadiazole containing PPV.
Hermona Christian[1], Subramanian Vaidyanathan[2], Changhee Ko[1], Rick Beyer[3] and Mary E. Galvin[1]; [1]Materials Science and Engineering, University of Delaware, Newark, Delaware; [2]Materials Research, Lucent Technologies, Murray Hill, New Jersey; [3]Multifunctional Materials Branch, WMRD, Army Research Laboratory, Aberdeen Proving Grounds, Maryland.

With polymers as the active layer on a plastic substrate, construction of flexible devices is possible, although the use of calcium cathodes places stringent requirements on the encapsulation of the device. Our work focuses on the development of polymers that will function with higher work function cathodes, making encapsulation less problematic. Additionally, we seek to fabricate stable, flexible PLEDs with a simple device configuration for military display applications. To this aim we have made efficient multi-layered flexible PLEDs using a statistical copolymer of hole transporting dialkoxy-substituted PPV with an electron transporting oxadiazole containing PPV derivative as the emissive layer. Even in single layered devices, this polymer shows good performance. When PEDOT/PSS was coated on the ITO and

LiF was evaporated between the emissive layer and Al, external quantum efficiency is significant improved to 1%. Several other cathode materials were also screened, and those results will be reported as well.

SESSION H2: Giant Area Electronics and Circuits
Chair: Virginia Chu
Thursday Afternoon, March 31, 2005
Room 2008 (Moscone West)

1:30 PM *H2.1
Flexible, Conformal, and Elastic Electronic Surfaces.
Sigurd Wagner, Electrical Engineering and PRISM, Princeton University, Princeton, New Jersey.

The display industry is beginning to manufacture on four-square-meter glass substrates, to supply the rapidly growing market for flat panel television sets. Within ten years, large area electronic surfaces will sell in the store for $ 1,000 or less per square meter. The arrival of manufacturing technology for low-cost giant integrated circuits is encouraging research into revolutionary concepts for electronic surfaces. Mechanical flexibility will be part of the next generation of display technology and eventually will enable surround displays. In the cards are conformally shaped sensors and displays, electronic textile circuits integrated by weaving, and elastic sensor and actuator skin. All of these already have been demonstrated in the lab. Giant electronics is shaping up as a rich area of research on the integration of electrical, optical, mechanical, and bio-chemical functions over large surfaces. These will need new electronic materials and fabrication processes, circuits, power supplies, communication and system architectures. I will discuss specific issues in materials, devices, and circuits for flexible, conformal, and elastic electronic surfaces.

2:00 PM H2.2
Lateral Nonuniformity And Mesoscale Effect in Giant Area Electronics. Victor G. Karpov, Diana Shvydka and Yann Roussillon; Physics and Astronomy, University of Toledo, Toledo, Ohio.

The recently developed physics of conventional giant area thin-film devices, such as terrestrial photovoltaics, is extended to the general field of giant area electronics. In particular, it has been established that large area, thin-film semiconductor structures often exhibit strong fluctuations in electronic properties on a mesoscale level that originate from relatively weak microscopic fluctuations in material structure such as grain size, chemical composition, and film thickness. Amplification comes from the fact that electronic transport through potential barriers is exponentially sensitive to the local parameter fluctuations. These effects create new phenomena and establish the physics of giant-area, thin-film devices as a distinctive field of its own. We show that (i) giant-area semiconductor thin-film devices are intrinsically nonuniform in the lateral directions, (ii) the nonuniformity can span length scales from millimeters to meters depending on external drivers such as light intensity and bias, and (iii) this nonuniformity significantly impacts the performance and stability of, e. g., flexible substrate photovoltaics, light-emitting arrays, and liquid-crystal displays. [1] In addition to the experimental data on lateral nonuniformity effects, we present a theoretical analysis based on the concept of random diode array proven relevant in describing a system of large number nonlinear interconnected elements. [2] In our work we derive a fundamental length scale that discriminates between the cases of small and large-area devices, and beyond which a new physics emerges. A new approach is developed to block the effects of lateral nonuniformities in thin-film semiconductor structures. Because the nonuniformity modulates the surface photo-voltage distribution, it generates laterally nonuniform electrochemical reactions when exposed to light and immersed in a proper electrolyte (red wine effect recently highlighted in the media). Such treatments result in a nonuniform interfacial layer that balances the original nonuniformity. This approach has been successfully implemented for photovoltaic devices where it improved the device efficiency from 2 % to 12%. [3] We feel that enhanced understanding of the effects of nonuniformities will help to improve the performance and stability in many giant area device applications. REFERENCES 1.V. G. Karpov, A. D. Compaan, and Diana Shvydka, Random diode arrays and mesoscale physics of large-area semiconductor devices, Phys. Rev B 69, 045325, (2004). 2.V. G. Karpov, Critical disorder and phase transition in random diode arrays. Phys. Rev. Lett., 91, 226806 (2003) . 3.Y. Roussillon, D. Giolando, Diana Shvydka, A. D. Compaan, and V. G. Karpov, Blocking thin film nonuniformities: photovoltaic self-healing, Appl. Phys. Lett. 84, 616. (2004)

2:15 PM H2.3
Fine-feature Patterning of Giant-area Flexible Electronics by Microcontact Printing and Digital Lithography.
William S. Wong, Michael L. Chabinyc, Eugene Chow, Rene Lujan, Juegen Daniel and Robert A. Street; Electronic Materials Laboratory, Palo Alto Research Center, Palo Alto, California.

The development of inexpensive high-performance electronics requiring low-temperature device processing would enable low-cost, giant-area flexible electronics for applications such as high-resolution giant-area displays, sensors, and evolving technologies such as electric paper. The spatial resolution, small drop volume and large-area coverage of jet-printing methods, combined with fine feature stamping and low-temperature semiconductor processing, is one approach for integrating high-performance thin-film transistors (TFTs) with giant-area flexible substrates. A novel digital-lithographic method, in which an electronically generated and digitally aligned etch mask is jet-printed onto a process surface, was used to fabricate hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) arrays. The digital lithographically fabricated arrays had features as small as 30 μm with 5 μm layer-to-layer registration and pixel resolution of 75 dpi over a four-inch diameter wafer. The resulting TFTs possessed on/off ratios of 10^8 and threshold voltages of 2-3 V. To further demonstrate the efficacy of the digital lithographic process, the technique has been applied to fabricate a-Si based TFTs backplanes on to flexible substrates. Given the ability for high-resolution spatial alignment, the digital lithographic process is ideal for registering multilayer patterns over a large-area flexible substrate in which localized alignment run out is a problem. In combination with digital lithography, a low temperature a-Si:H based TFT deposition process (T$\sim$170°C) was used to fabricate TFT devices having threshold voltages of 4 V and on/off ratios of 10^8 and carrier mobility of 0.9 cm^2/V·s, comparable to conventional a-Si:H TFT devices. The same process was used to make 128×128 pixel matrix addressed TFT arrays having 75 dpi resolution on polyimide and polyethylene napthalate flexible substrates. Device characteristics for the low-temperature TFT arrays on flex will be presented and compared to devices created by conventional methods. In order to achieve smaller pattered features, the digital lithography process has been combined with micro-contact printing methods in order to pattern TFT device structures with channel lengths as short as 5 microns. In this process, a poly(dimethylsiloxane) stamp was used to pattern fine feature masks within a pixel and digital lithography was used to pattern the features for the giant-area electronics. We will present various techniques for all print patterned giant-area electronics. All jet-print patterned TFT pixel designs having a minimum feature size of < 10 microns and integration of the flexible TFT array backplane with electrophoretic display media will also be discussed.

2:30 PM H2.4
Development of PVDF Thick Film Interdigitated Capacitors for Pressure Measurement on Flexible Melinex Substrates.
Khalil Ibrahim Arshak[1], Arousian Arshak[2], Deirdre Morris[2], Olga Korostynska[1], Essa Jafer[1], John Harris[1] and Seamus Clifford[1]; [1]Electronic and Computer Engineering, University of Limerick, Limerick, Munster, Ireland; [2]Physics, University of Limerick, Limerick, Munster, Ireland.

Thick film strain gauges are used in many areas including automotive, aerospace, robotics and biomedical applications. This popularity is mainly due to their rugged nature, cost effectiveness and reproducibility. Furthermore, thick film technology allows the use of a wide range of materials and structures, so that sensors with the desired physical properties can be obtained(1). In this study, the behaviour of a PVDF thick film paste was evaluated as a strain gauge on alumina substrates and as a pressure sensor on flexible Melinex substrates. PVDF was chosen due to its versatility and relatively non-toxic properties, making it suitable for a wide range of applications. The thick film paste was prepared by mixing PVDF with 7 wt.% Ethyl Cellulose (binder), 1 wt.% Lecithin (surfactant) and Terpinol-α, which was the solvent used to form a paste. Using the screen-printing process, silver interdigitated electrodes were deposited. Following this, three layers of PVDF paste were printed. An interdigitated structure was chosen as it contains no moving parts and requires one less process step than a sandwich structure. Changes in pressure or strain result in a deformation of the dielectric layer(2). After printing, samples were dried at 100°C for a half hour and then cured at a peak temperature of 170°C. Samples on alumina substrates were placed in a cantilever beam arrangement so that their piezocapacitive effect could be measured. The gauge factor is calculated from the slope of the graph showing the change in capacitance, ΔC, over the original capacitance, C, against the applied strain. Sensors were found to exhibit a gauge factor of 6.2, which is higher than that the 3.5 previously reported for thick film PVDF gauges using a sandwich structure(3). Furthermore, the gauge exhibited a hysteresis of less than 0.1 %. Sensors on Melinex were then mounted on planar and cylindrical substrates and subjected to hydrostatic pressure in the range of 0$-$14 kPa. In this case, ΔC/C was plotted against the pressure. A linear response was obtained in both cases, with the capacitance more than doubling over the entire pressure range. It was also found that, samples on cylindrical substrates showed a slightly higher response than those on planar substrates. Both planar and cylindrical samples showed a low hysteresis. However, the repeatability error is increased for sensors on cylindrical substrates. XRD, SEM and optical microscopy are used to examine the crystalline phase and microstructure of the PVDF films on various substrates. These techniques are also used to examine changes in phase and the onset of ductile or brittle behaviour due to mechanical deformations induced through the application of pressure and repeated cycling. 1. Newman, M.R., et al., IEEE Engineering in Medicine and Biology Magazine, 1994. 13(3): p. 409-419 2. Filanc-Bowen, et al., Proceedings of IEEE Sensors, 2002. 2: 1648-1653 3. Arshak, K., et al., Sensors and Actuators A, 2000. 79: p.102-114

3:00 PM H2.5
Fully Integrated High Frequency Nanowire Ring Oscillators.
Robin Sean Friedman[1], Michael C. McAlpine[1], David S. Ricketts[2], Donhee Ham[2] and Charles M. Lieber[1,2]; [1]Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts; [2]Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

Macroelectronic circuitry implemented on non-crystalline substrates such as glass and plastic holds the promise of making computing devices ubiquitous due to their light weight, flexibility, and low cost. However, the temperature restrictions imposed by these substrates restrict the use of high carrier mobility materials, such as polycrystalline silicon, generally limiting these devices to the modest computational capabilities of amorphous silicon and organic semiconductor thin film transistors (TFTs). Densely assembled films of single-crystal, semiconducting nanowires, which have been shown to function as active components in high mobility TFTs, can be fabricated via an ambient temperature process on virtually any substrate. Key to determining the viability of such structures in applied circuitry is the demonstration of fully interconnected devices which can operate under high speed conditions and generate self-sustained, high frequency waveforms; previous work has only demonstrated unintegrated devices under direct current (DC), time invariant conditions. While recent work suggests that single carbon nanotube transistors can function under high frequency alternating current (AC) conditions, previously demonstrated unintegrated ring oscillators composed of these transistors displayed frequencies of only several hundred hertz. Here we report the fabrication of integrated systems of high-performance TFTs made from dense, patterned Si nanowire films on both Si and glass substrates. We show that these systems can function as logical inverters with gain under both DC and AC conditions up to megahertz frequencies. On-chip integration of multiple inverters allows for the generation of ring oscillators with frequencies up to 11.7 MHz, the highest observed frequency for circuits based on nanoscale materials.

3:15 PM H2.6
Poly(3-Hexylthiophene) Organic Thin Film Transistor on Polyimide using Electroplated Au Electrodes.
J. G. Lee, Y. G. Seol and Nae-Eung Lee; Materials Engineering, Sungkyunkwan University, Suwon, Kyunggi-do, South Korea.

Organic thin film transistors (OTFT) on flexible substrate utilizing electroplated Au electrodes have potential advantages in the fabrication of flexible devices requiring large area coverage, structural flexibility, low-temperature processing, and especially low cost. In particular, the application of electroplated electrode with the adhesion layers enables one to obtain reliable devices on the flexible substrate in terms of mechanical flexibility and thermal stability, as proved in the flexible printed circuit board (FPCB) technology. In this work, poly(3-hexylthiophene) (P3HT) OTFT devices with top and bottom gate structures were fabricated with electroplated Au source/drain (top gate structure) or gate electrodes (bottom gate structure). First, since the adhesion of electrodes on the flexible substrate is of great importance for the application in flexible devices, the adhesion improvement of electroplated electrode structures was investigated by plasma treatment of polyimide substrate in Au/Cu/Cr/polyimide structures. Cu(seed)/Cr(adhesion) layers were sputter-deposited in sequence on the plasma-treated polyimide substrate. Then, a negative photoresist, SU-8, was spin-coated on the Cu/Cr/polyimide substrate and patterned by ultra-violet photolithography for electrodes. After photolithography, Au source/drain or gate electrodes were electroplated into the patterned SU-8 mask. For the top gate structure, after SU-8 ashing and Cr/Cu layer removal, spin-coating of P3HT layers, SiO_2 gate dielectric the evaporation, and Al electrode deposition were carried out with a shadow mask. For the bottom gate structure, after the formation of electroplated Au gate electrode, SiO_2 gate dielectric deposition, gold source/drain evaporation, and P3HT spin-coating were carried out in sequence. The channel length ranged between 5 and 110 μm, and the channel width was 800 μm. Electrical properties of fabricated OTFTs were characterized and the effect of various process conditions and structures on the performances of fabricated devices will be discussed.

3:30 PM H2.7
Nanocrystalline Silicon Thin Film Transistors on Optically Clear Polymer Foil Substrates.
Alex Kattamis[1,2], I-Chun Cheng[1,2], Ke Long[1,2], James C. Sturm[1,2] and Sigurd Wagner[1,2]; [1]Department of Electrical Engineering, Princeton University, Princeton, New Jersey; [2]Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton, New Jersey.

Flexible displays are the next technology generation for flat-panel displays. Therefore interest is growing in building high-performance thin-film transistor (TFT) backplanes on clear flexible substrates. Ideally, a flexible backplane should be constructed using fabrication processes already developed for glass with only minor changes. Nanocrystalline silicon (nc-Si:H) TFTs have at least ten times the ON current of amorphous silicon TFTs and can be plasma deposited at temperatures in upwards of 150°C. We have fabricated nc-Si:H TFTs on temperature resistant polymer foil substrates, first on orange colored Kapton® 200E, and now on a clear polymer. Organic polymer substrates may be processed either mounted on a rigid holder, to ensure dimensional stability, or free-standing. We are working with both methods, but here the focus is on free-standing substrates. Both these substrates have high glass transition temperatures and are therefore candidates for direct substitution of display glass. This introduces the next challenge, overcoming the effects due to the mismatch in coefficients of thermal expanstion (CTE) between silicon TFT materials and the polymer substrates. The effects of mismatch become more pronounced as process temperature increases. This mismatch, and built-in stresses in the device films, can combine to fracture TFT structures during processing. We demonstrate techniques that are available for avoiding device and substrate fracture. We fabricated nc-Si:H TFTs at 150°C to 200°C on a clear polymer (CTE = 45 to 55 ppm/K), on Kapton® 200E (CTE = 17 ppm/K), and on 1737 glass (CTE = 4 ppm/K) for comparison. Stress developed in device layers was compensated by designing stresses, via PE-CVD growth conditions and layer thicknesses, into the silicon nitride films that serve to passivate the front and back of the polymer substrate. The stress in the substrate was decreased by reducing device layer thicknesses and by cutting the device layers into islands separated by exposed polymer. By using these three techniques we have made directly deposited nc-Si:H TFTs on clear polymer foils with electron mobilities of up to 15 cm^2/Vs.

3:45 PM H2.8
ZnO Thin Film Transistors on Gate Dielectrics Grown By Atomic Layer Deposition.
Peter F. Carcia[1], Robert Scott McLean[1], Michael H. Reilly[1], Yoshi Senzaki[2] and S. G. Park[2]; [1]Research and Development, DuPont, Wilmington, Delaware; [2]Aviza Technology, Scotts Valley, California.

Investigation of large area electronics on low-temperature, flexible substrates frequently focuses on limitations of the semiconductor, especially its too low mobility. In fact many applications, such as pixel-select transistors in a display, require only a modest mobility (< 1 $cm\hat{2}/V$-s). More often it is the poor performance of the gate dielectric that is more limiting, i.e. high leakage current or high interface trap density, responsible for high threshold voltage. In the IC industry, where there is a need to replace the thermally grown SiO2 gate dielectric in the highest performance transistors, atomic layer deposiiton (ALD) is emerging as the preferred method for growing dense, pinhole-free, high performance gate dielectric films. While ALD films are commonly grown at moderate substrate temperature (> 300 C), introduction of new precursor chemistry and plasma-assist have reduced, and for some materials, eliminated the need for substrate heating, making ALD attractive for low-temperature plastic substrates. In this paper we compare ZnO thin film transistor (TFT) properties on gate dielectrics of Al2O3, HfO2, and HfSiO2 grown by ALD with corresponding properties on thermally grown SiO2. Specifically for HfO2, ZnO TFTs had mobility >10$cm\hat{2}/V$-s, Vth = 2.5V, and a subthreshold slope $\sim$ 0.5 V/decade. This represents a 40x increase in mobility and a 10x reduction in Vth compared to ZnO TFTs simultaneoously grown on SiO2 gate dielectric. Further, we will discuss the effect of ALD growth temperature of gate dielectrics on ZnO TFT properties and the implications for large area electronics on plastic substrates.

4:00 PM H2.9
Temperature Dependence of I-V Characteristics of Organic PN Diodes and Their Application to Sheet Thermal Sensors.
Yusaku Kato[1], Tsuyoshi Sekitani[1], Shingo Iba[1], Takayasu Sakurai[2] and Takao Someya[1]; [1]Quantum-Phase Electronics Center, The University of Tokyo, Tokyo, Japan; [2]Center for Collaborative Research, The University of Tokyo, Tokyo, Japan.

We have fabricated organic pn diodes on plastic films and measured temperature dependence of I-V characteristics in the wide range from

30 to 240°C under N_2 environment. The current (I_F) was increased by a factor of 20 with changing the measurement temperatures from 30 to 160°C where I_F was monitored at forward voltage bias of 2 V. Furthermore, temperature dependence of I-V curves was reversible and reproducible when the measurement temperature was below 160°C. This result shows the feasibility of organic pn diodes for thermal sensor applications. Organic pn diodes have been manufactured on an ITO-coated poly(ethylene naphthalate) (PEN) film (98 Ω/, Teijin Dupont Films) with thickness of 200 μm. First, the surface of the ITO-coated base films were cleaned by organic solvent in the ultrasonic bath and exposed to ozone (3 min, room temperature). Then, 30-nm-thick copper phthalocyanine (CuPc, p-type) and 50-nm-thick 3,4,9,10-perylene-tetracarboxylic-diimide (PTCDI, n-type) were deposited by vacuum evaporation (5~9 x 10^{-5} Pa, ~3 nm/min). Subsequent processes have been performed without exposure to air. After depositing organic layers, the film was transferred to glove box (<1 ppm O_2 and H_2O), where a metal mask for cathode was attached to the film, and then loaded into a vacuum chamber, again. Finally, 150-nm-thick gold was deposited as cathode by vacuum evaporation. The size of cathode was 450 x 450 μm^2. Prior to measurements of the temperature dependence, the I-V characteristics of the pn diodes at room temperature were measured with a semiconductor parameter analyzer (Agilent, 4156C). All the measurements were performed in the glove box without exposure to light. The current density was 200 mA/cm^2 at 2 V bias and 0.03 mA/cm^2 at -2 V. The breakdown and the threshold voltage were -17 V and 4 V, respectively. Then temperature dependence of I-V characteristics was measured. The current density at 2 V bias was enhanced from 200 mA/cm^2 to 4 A/cm^2 when the measurement temperature changed from 30 to 160 °C, namely twentyfold enhancement of measured currents. This tendency can be fitted by Arrhenius's formula, indicating a carrier transport of thermal excitation. The evaluated activation energy was 0.5 eV. Furthermore, temperature dependence of I-V curves was reversible and reproducible after many heat cycles from 30 up to 160 °C. We have recently reported a flexible, large-area pressure sensor with an OFET active matrix for electronic artificial skin (E-skin) applications.[1] The present study shows feasibility of organic pn diodes as thermal sensors, which are flexible, lightweight, potentially ultra low in cost even for large area and furthermore compatible with manufacturing process of OFETs. Therefore, we believe that the organic diode should be the strong candidate for large-area thermal sensors for E-skin implementation. The authors thank MEXT IT program and COE program for financial supports. [1]T. Someya, et al, PNAS, **101**, 9966 (2004).

SESSION H3: Organic Photonics and Electronics for Large Area Substrates and Flexible Displays

Chair: Martin Stutzmann
Friday Morning, April 1, 2005
Room 2000 (Moscone West)

9:00 AM *H3.1
Status and Opportunities for High Efficiency OLED Displays on Flexible Substrates. Michael Hack[1], Anna Chwang[1], Yeh-Jiun Tung[1], Richard Hewitt[1], Julie Brown[1], JengPing Lu[2], Chinwen Shih[2], Jackson Ho[2], R. A. Street[2], Lorenza Moro[3], Xi Chu[3], Todd Krajewski[3], Nicole Rutherford[3] and Robert Visser[3]; [1]Universal Display Corporation, Ewing, New Jersey; [2]Palo Alto Research Center, Palo Alto, California; [3]Vitex Systems, Inc., San Jose, California.

Organic Light Emitting Device (OLED) technology is now proving itself as an ideal media for the implementation of bright, high information content, video rate, flexible displays. Recent advances in the development of phosphorescent OLEDs (PHOLED™) enable the development of advanced mobile communication devices requiring very low power consumption. In this paper we will outline our progress towards developing such a low power consumption active-matrix flexible OLED (FOLED™) display. Our work in this area is focused on three critical enabling technologies. The first is the development of a high efficiency long-lived phosphorescent OLED (PHOLED™) device technology, to enable the low power consumption performance requirements for mobile display applications. Secondly, is the development of flexible active-matrix backplanes to drive PHOLED front-planes, and for this we consider poly-Si TFTs formed on metal foil substrates as this approach represents an attractive alternative to fabricating poly-Si TFTs on plastic for the realization of first generation flexible active matrix OLED displays. Thirdly, the key to reliable operation is to ensure that the organic materials are fully encapsulated in a package designed for repetitive flexing. In collaboration with Vitex, UDC is developing long-lived flexible OLED displays based on using multi-layer, thin film barrier and encapsulation.

9:30 AM H3.2
High-Mobility Pentacene-Based Transistors on Plastic Substrates. Siddharth Mohapatra[1], Michelle Grigas[1], Robert Wenz[1], Robert Rotzoll[2], Viorel Olario[2], Oleg Shchekin[1,3], Klaus Dimmler[2] and Ananth Dodabalapur[1,3]; [1]Organic ID, Austin, Texas; [2]Organic ID, Colorado Springs, Colorado; [3]The University of Texas at Austin, Austin, Texas.

Organic field-effect transistors (OFETs) are being developed for several electronic applications including flexible displays, biological and chemical sensors, and RFID (radio frequency identification device) tags. To explore the full range of advantages offered by organic electronic materials it is important to be able to manufacture high-performance electronics on flexible substrates at very low cost. Also, to be usable in such relatively high-performance applications as RFID tags, the polymer-based OFETs will have to have mobility ~ 0.3 cm2/V-s and channel lengths on the order of a few microns. To achieve such performance it is necessary to optimize the dielectric surface on which pentacene is deposited as well as the injection of carriers into the conduction channel. The paper presents a method for achieving high mobilities in pentacene-based organic film-effect transistors (OFETs) on plastic substrates. These transistors are part of a two-level metal-based organic electronic circuit technology. The fabrication process also includes a critical step which consists of dielectric surface cleaning using gas plasma or ozone, followed by application of various self-assembled monolayer (SAM) materials such as octyl trimethoxy silane (OTS) or hexamethyldisilane (HMDS). Pentacene is purified and evaporated in vacuum with the substrate maintained at room temperature. The devices with HMDS repeatedly exhibit highest mobility on the order of 1 cm2/V-s and on-off ratios up to 103. The devices have a channel length in the range 2-4 mm. Devices with HMDS and OTS have mobilities higher than those without any dielectric cleaning or surface treatment, but exhibit more pronounced hysteresis in the Id vs. Vgs characteristics. The relatively poor performance of the untreated devices may be attributed to the surface contamination with chemicals used during circuit preparation. The performance of simple electronic circuits such as inverters and rectifiers fabricated using the aforementioned mobility-enhancing techniques is also discussed.

9:45 AM H3.3
Polymer Light Emitting Diodes with Layer-by-Layer Structure Prepared by ESDUS Method. Katsuhiko Fujita, Takamasa Ishikawa and Tetsuo Tsutsui; Graduate School of Engineering Science, Kyushu University, Kasuga, Fukuoka, Japan.

We have reported a new type of polymer ultra-thin film preparation method, the spray deposition, and the application for organic optoelectronic devices such as an organic light emitting diode (OLED). In this method, a highly diluted solution of an organic material is nebulized into air and concentrated under a controlled evaporation condition. The resulting aerosol is transported by a carrier gas and deposited onto a solid substrate. This method has substantial advantages that an almost insoluble and non-evaporative material can be fabricated into a thin film, and that a separate-coating and layer-by-layer structure of polymers can be performed. An OLED was prepared from highly diluted THF solutions, below 1 ppm, of two poly-phenylenevinylene derivatives. One shows red emission and the other green. The red polymer was deposited on an ITO electrode through a shadow mask with round holes and 0.1 mm line width to result a fine separate-coating and the green one was deposited onto the patterned film. An Al anode was deposited on the polymer film in a vacuum evaporator. The fabricated OLED showed a patterned emission at around 10 V.

10:30 AM H3.4
A Novel Patterning Technique for High-Resolution RGB-OLED-Displays: Laser Induced Local Transfer (LILT). Michael Kroeger[1], Thomas Dobbertin[1], Henning Krautwald[2], Thomas Riedl[1], Hans-Hermann Johannes[1,2] and Wolfgang Kowalsky[1,2]; [1]Institut fuer Hochfrequenztechnik, Technische Univ. Braunschweig, Braunschweig, Germany; [2]Labor fuer Elektrooptik, Technische Univ. Braunschweig, Braunschweig, Germany.

A novel technique for high-resolution patterning of organic semiconductors is presented. There are mainly three different approaches of realizing full-colour OLED-displays (OLED: organic light emitting diode). One of these is colour from white by applying a colour-filter-matrix to a white-light emitting OLED-display. Another approach is to convert blue light into green and red light by a colour-converting phosphor matrix (colour from blue). Micro-patterning of red, green and blue OLEDs is to be favoured for reasons of lower costs and higher efficiency. Common patterning techniques implying photolithography cannot be applied to OLEDs due to their strong degradation upon exposure to solvents. A first generation of RGB-OLED-displays was patterned by shadow masking.

If bigger substrate sizes of future mass production tools are considered, shadow masking may not fit the requirements, as the mechanical stability of the mask itself will be a problem. Taking this into account alternative patterning techniques have to be developed. In the past we demonstrated a local sublimation method [1], where a Mo-film was deposited onto a thin polyimid-foil (PI) and patterned by photolithography giving thin stripes. Onto the opposite side the desired organic material was deposited by organic molecular beam deposition (OMBD). By heating the Mo-stripes with short high current pulses the organic material could be sublimed locally, which then deposits onto an OLED substrate placed in a short distance from the PI-foil. In this work we demonstrate a local sublimation method for which the resistive heating was replaced by a radiative heating performed by a focussed infrared laser beam. An infrared absorbing substrate (target) is coated with either a red, green or blue light-emitting organic material and placed in a short distance (below 50 μm) of the OLED-substrate onto which the organic material is to be patterned. The laser beam is deflected by a scanner onto the target in single lines. If the scanning speed and the laser power are adjusted properly, the target locally heats up to a temperature at which the organic material sublimes and condenses on the opposing OLED-substrate. By repeating this process for each colour red, green and blue stripes can be deposited in with widths below 300 μm. As next step a RGB-patterning-tool designed for inline-processing of OLED-displays has been built. First results of RGB-OLEDs patterned by this tool are to be discussed. References: [1] E. Becker, T. Riedl, T. Dobbertin, D. Schneider, D. Heithecker, D. Metzdorf, H.-H. Johannes, W. Kowalsky, Appl. Phys. Lett. 2003, 82, p. 2712

10:45 AM H3.5
Direct 110 Volt, 60 Hertz Operation of Organic Light Emitting Devices. Jason Slinker[1], John DeFranco[1], Jonathan Rivnay[1], Samuel Flores-Torres[2], Hector Abruna[2] and George Malliaras[1]; [1]Materials Science and Engineering, Cornell University, Ithaca, New York; [2]Chemistry and Chemical Biology, Cornell University, Ithaca, New York.

Ionic transition metal complexes are receiving increased attention due to the high efficiency obtained in organic light emitting devices with air-stable cathodes. We report on devices based on ruthenium(II)-tris-bipyridine complexes that can be sourced directly from a standard U.S. wall outlet. With the aid of the ionic liquid 1-butyl-3-methylimidazolium, these devices show sufficiently fast response time to switch at frequencies up to 120 Hz. Fabricated from a single spin cast organic layer, these devices are prepared in a sandwich-structure cascaded architecture. This architecture sustains high input voltages, provides fault tolerance, and facilitates the fabrication of large area solid-state lighting panels.

11:00 AM H3.6
Reflective Displays with Giant-area Compatible Backplanes. Jurgen H. Daniel, Brent Krusor, William Wong, Ana Arias, Rene Lujan, Raj Apte and Robert Street; EML, PARC, Palo Alto, California.

In the future information will be displayed not only on rigid monitors, but displays will be found embedded in walls, furniture, clothes, or they may appear as roll-up displays similar to the way sheets of paper can be rolled up. Some of these displays will require large-area or giant-area electronic backplanes. Flexibility, low cost and low power consumption are amongst some of the requirements for such displays, often referred to as electric paper. Electrophoretic ink technology is promising for reflective displays with paper-like appearance. For giant-area display backplane electronics conventional semiconductor processes such as lithography and vacuum deposition may become too costly. Direct-writing techniques such as jet printing can be used as a viable alternative. Here we report on flexible electrophoretic media and the integration with various backplanes technologies. The electrophoretic medium is based on micro-cell structures which are fabricated using photolithography or potentially cheaper molding techniques. The substrate is Mylar foil coated with transparent conductive indium-tin-oxide (ITO). Typically, the cell structures are about 200 microns square and about 50 microns tall. After filling the cells with electrophoretic ink they are sealed with an overcoated polymer film. The electrophoretic medium is then laminated to the backplane. We have demonstrated ultra-flexible directly addressed electrophoretic displays. However, active matrix addressed displays offer a greater value. Particularly, active matrix backplanes, made by jet printing techniques are promising for potentially inexpensive flexible displays. In one approach a novel digital-lithographic method, in which an electronically generated etch mask is jet-printed onto a process surface, was used to fabricate amorphous silicon (a-Si:H) thin-film transistor (TFT) backplanes with a pixel resolution of 75dpi. In another approach the a-Si:H semiconductor material was replaced with a jet printed organic semiconductor. Due to the larger feature sizes of the printing technique compared to conventional lithography a reduced fill factor can occur and its effect on the image quality was investigated. The integration of the electrophoretic medium with the backplane also poses challenges such as the uniformity, the flexibility and the thickness of the glue layer between the media and the backplane. Using a lamination technique we were able to achieve thin glue layers with good thickness uniformity. Furthermore, impurities in the sealing layer or in the glue layer can cause a loss of resolution in the displayed image. We have studied this effect and first results will be presented.

11:15 AM H3.7
The Polymer/Anodized Al_2O_3 Hybrid Gate Dielectrics of OFET for Flexible Display. Kwonwoo Shin, Sang Yoon Yang and Chan Eon Park; Chemical Engineering, Pohang University of Science and Technology, Pohang, Gyungbuk, South Korea.

In the study of organic field effect transistors, the formation of good gate dielectric layer is one of the most important processes when being fabricated on the flexible substrate. Until now, the study on the formation of gate dielectrics has been focused on using cross-linked polymers or inorganic materials. But, in our research, we used both inorganic materials and polymer materials to enhance the performance of the gate dielectric layer. Also, we used neither any high temperature processes nor vacuum equipments for making our gate dielectric layer. Our gate dielectric layer consists of anodized Al_2O_3 layer and spin-coated Poly(methyl methacrylate)(PMMA) layer. By anodizing the surface of aluminum electrode used as gate electrode, we could make Al_2O_3 passive thin film on the aluminum gate electrode. This passive film had very good insulating and dielectric properties. So it could reduce the leakage current and increase the capacitance of dielectrics. And the additional thin PMMA coating on the anodized Al_2O_3 could reduce the surface roughness and surface energy of dielectrics. The OFETs having layered PMMA/Al_2O_3 gate dielectrics showed high performances. The OFETs on the flexible polyimide substrate showed 0.3 cm^2/Vs of mobility, 10^7 of on/off ratio, 0.8 V/decade of subthreshold slope and the OFETs on the SiO_2 substrate showed 1 cm^2/Vs of mobility, 10^7 of on/off ratio, 0.9 V/decade of subthreshold slope. The ordering of pentacene was dependent on the surface roughness and surface energy of our dielectrics. The vertical and horizontal orderings of pentacene were investigated with X-ray diffraction and the orientation of pentacene molecules on the dielectric surface was investigated with Near Edge X-ray Adsorption Fine Structure (NEXAFS) in Pohang Accelerator laboratory in Korea.

11:30 AM H3.8
Encapsulation of Flexible Organic Light-Emitting Diodes using Photocurable Coatings and Polyvinylidene Chloride (PVDC). C. S. B. Ruiz[1], Rodrigo F. Bianchi[1], Ely Antonio Tadeu Dirani[1,2], Fernando Josepetti Fonseca[1] and Adnei Melges de Andrade[1]; [1]PSI, Escola Politecnica/USP, Sao Paulo, Sao Paulo, Brazil; [2]FTMT, Pontificia Universidade Catolica de Sao Paulo, Sao Paulo, Sao Paulo, Brazil.

One of the most promising display technologies to come along the last decades is the organic light-emitting diodes (OLEDs). They have potential to be produced on large flexible substrate that would enable processing in a roll-to-roll manner. However, as the organic material is very susceptible to water vapor and oxygen, thorough encapsulation is indispensable, which is crucial to performance and lifetime of the polymer display. Moreover, the barriers coatings requirements for such flexible devices must exhibit good adhesion to the display surface, as well as it must not damage their active components. In this work we have investigated the use of photo curable coatings (urethane aliphatic diacrylate resin, 1,6 hexanodiol diacrylate monomer, photoinitiator, light stabilizer HALS and UV absorber) and polyvinylidene chloride (PVDC) films as protective layers of flexible light-emitting diodes based on poly (2-methoxy-5- (2 ethyl-hexyloxy) p-phenylene vinylene) - MEH-PPV. The material coatings were applied onto the bottom and top of a typical device structure (PET/ITO/MEH-PPV/Al), and the electrical and optical characteristics of the OLEDs were examined as function of light exposure time in air. The improvement of the lifetime, as well as the excellent adherence of the coatings on the flexible substrate, on the cathode and on polymer emissive layer shows the potential for such class of barrier materials to be used in OLEDs. This work was sponsored by Fapesp, CNPq and IMMP/MCT.

11:45 AM H3.9
Pentacene Field-effect Transistors with 230-nm-thick Polyimide Gate Dielectric Layers. Shingo Iba[1], Tsuyoshi Sekitani[1], Yusaku Kato[1], Takayasu Sakurai[2] and Takao Someya[1]; [1]Quantum-Phase Electronics Center, School of Engineering, The University of Tokyo, Tokyo, Japan; [2]Center of Collaborative Research, The University of Tokyo, Tokyo, Japan.

We have fabricated pentacene field-effect transistors (FETs) with 230-nm-thick polyimide gate dielectric layers cured at 180°C on polyethylene naphthalate (PEN) film. With the source-drain bias of -8 V, the transistors showed field effect mobility of 0.13 cm^2/Vs, the on/off ratio of 10^7 and the subthreshold swing of 1.7 V/decade. Pentacene FET's (top contact geometry) with polyimide gate dielectrics of thickness from 230 nm to 970 nm were fabricated. First, a 5-nm-thick chromium adhesion layer and a 50-nm-thick gold layer were deposited through shadow masks to form gate electrodes on PEN film. Then, polyimide precursors were spin-coated and cured at 180°C for 1 hour. To form polyimide gate dielectric layers of various thicknesses, the rotation velocity during spin coating and the viscosity of polyimide precursors were systematically changed. Pentacene was purified by the vacuum sublimation method and deposited in the vacuum system to form a 50-nm-thick layer. Subsequently, the samples were transferred, without exposing to air, to the glove box (O_2 and H_2O < 1 ppm), where the metal masks were placed onto the film. After loading the samples into the vacuum system, a 60-nm-thick gold layer was deposited to form source and drain electrode on the top of the pentacene layer. The channel width W and length L are 1.6 mm and 50 μm respectively. The device characteristics were measured with a semiconductor parameter analyzer (Agilent 4156C) in the glove box. When source-drain voltage V_{DS} = -8 V was applied to the transistor with a 230nm-thick dielectric, the field effect mobility in saturation region was 0.13 cm^2/Vs, the on/off ratio was 10^7 when off current was defined as minimum drain current I_{DS} at positive gate bias. The subthreshold swing was 1.7 V/decade. Field-effect mobility in saturation region increases with increasing gate bias V_{GS} and reached0.5 cm^2/Vs at the gate voltage of -40 V. In case of transistor with a 670-nm-thick dielectric, the mobility was 0.08 cm^2/Vs, the on/off ratio was 10^6 when a drain voltage V_{DS} of -8 V was applied. These characteristics are comparable to the reported characteristics of the pentacene devices with polyvinylphenol (PVP) gate dielectrics.[1] These results demonstrate feasibility of low voltage operation of flexible organic FETs with polyimide gate dielectric layers,[2] which would be a key technology for large area sensor sheets like electronic artificial skin (E-skin).[3] The authors thank MEXT IT program and COE program for financial supports. [1] Hagen Klauk, *etal*, J. Appl. Phys. **92**, 5259 (2004). [2] Yusaku Kato, *etal*, Appl. Phys. Lett. **84**, 3789 (2004). [3] T. Someya, *etal*, Proc. Natl. Acad. Sci. U.S.A. **101**, 9966 (2004).

SESSION H4: FETs, MEMs, Biochips, and Photovoltaics for Giant Area Electronics and Photonics

Chair: Stephanie Lacour
Friday Afternoon, April 1, 2005
Room 2000 (Moscone West)

1:30 PM *H4.1

Thin-film Biochips. Virginia Chu[1], Filipa Fixe[1,2], Duarte Miguel Prazeres[2] and Joao Pedro Conde[1,3]; [1]INESC MN, Lisbon, Portugal; [2]Center of Biological & Chemical Engineering, Instituto Superior Tecnico, Lisbon, Portugal; [3]Department of Chemical Engineering, Instituto Superior Tecnico, Lisbon, Portugal.

The widespread application of biochips in applications such as genetic analysis, pathogen identification and expression analysis requires inexpensive fabrication and simple, reliable diagnostics. The integration of electronics with biology has great potential in these areas. Large area electronics, based on hydrogenated amorphous silicon, nanocrystalline silicon and polycrystalline silicon processed at low temperatures (T<400 °C), which is the basis of the electronic backplane of the flat panel LCD display, provides a technology that can allow functional electronic devices to be integrated into biochip applications. The low temperature processing, characteristic of thin film technology, allows the use of a wide variety of substrates such as glass (large area and low cost), plastic (flexible and low cost) and biocompatible materials. In the present work, thin film microelectronics technology is used to create a DNA chip platform with 2 main features: (1) integrated metal electrodes allow the electronic addressing of DNA probes and targets and (2) an integrated amorphous silicon photodetector allows on-chip detection of tagged DNA strands. Single square voltage pulses are used to enhance the rate of covalent immobilization and hybridization of single stranded DNA probes on a chemically functionalized thin film surface (silicon dioxide) by 7 to 9 orders of magnitude. The pulse is applied to integrated metal electrodes (voltage and ground lines) incorporated below the functionalized thin film surface on a polyimide substrate. These metal electrodes have dimensions that range from a few microns to a few millimeters. The DNA chip structure was also fabricated on a glass substrate integrating a thin-film, multi-layered, optoelectronic detector based on a-Si:H. This detector was for the quantitative optoelectronic detection of immobilized and hybridized DNA. This device, which relies on the labeling of DNA molecules with the fluorophore PyMPO, can detect surface concentrations down to 1 pmol per square centimeter. Recent results expanding the concepts of electric-field-assisted reaction rate control to thin-film protein-chip applications, as well as new developments regarding the electromechanical detection of unlabeled DNA hybridization using thin-film MEMS and the fully electronic detection of biomolecules using electrolyte-gate thin-film transistors will also be presented.

2:00 PM *H4.2

Flexible Solar Cells for Integration with Textiles.
Markus Schubert, Institute of Physical Electronics, University of Stuttgart, Stuttgart, Germany.

Ubiquitous computing requires ubiquitous and mobile power supply. Since modern portable electronic equipment greatly benefits from Moore's law which also scales down the power demand of steadily shrinking circuits, we experience the emerging chance of providing the necessary mobile electric power by solar cells, integrated with portable phones, handheld computers, autonomous sensor and surveillance systems, smart tags etc. The power density of ambient light, and hence photovoltaic power from restricted area, is severely limited. We therefore pursue an approach of integrating flexible solar cells with larger area textiles, clothing and various types of garments and accessories. This contribution presents the development and current status of flexible solar cells for textile and clothing integration. The temperature for direct deposition on thin polymer foils which are suited for textile integration is generally limited to about 110°C. At present, the only choice of material which meets this requirement is amorphous silicon. Such low temperature cells need careful optimization of doped layers and light trapping. Their conversion efficiency is limited to 5%. But still, protocrystalline silicon absorber layers from very high frequency deposition and optimized hydrogen dilution are mandatory for achieving such values. In contrast, the transfer of thin monocrystalline silicon cells to plastic foils opens an efficiency potential around 15%, thus clearly outperforming amorphous silicon-based cells, even under low-light conditions. Our laboratory results reach up to 14.6% from a 25-micron thin, monocrystalline cell of 4 cm^2 area. In order to predict the performance of different clothing integrated photovoltaic materials, we model and measure their energy yield under a wide range of illumination spectra and intensities. Moreover, a mobile current/voltage-analyzer tracks solar cell characteristics under real application conditions. A brief review of first professional prototypes of clothing integrated photovoltaics which were realized with partners from clothing industry concludes this presentation.

2:30 PM H4.3

A Comparison of Additive Solution Processed Organic Channel FETs with Silicon Substrate Reference Devices.
Ian Sage, Wendy Howie, Jonathan Hughes, Paul Rose, Rachel Tuffin and Isabelle Votte; Photonics & Displays, QinetiQ Ltd, Malvern, United Kingdom.

This paper reports the properties of bottom gate organic channel FET devices fabricated on a silicon substrate, with a silica dielectric and vacuum deposited source and drain electrodes. A comparison is then made with devices in which the inorganic layers of the FET are progressively substituted by solution processed materials, en route to a fully printed electronic system. Our processing route has the following features: - All electronically active layers are built up on a plain, unpatterned substrate - No vacuum deposition processes are required at any stage - The processing is exclusively additive, with no etch, dissolution or photolithography processes - All the steps are compatible with processing on conformal and flexible substrates - Low temperature processes compatible with plastic substrates are used throughout We have chosen a hybrid fabrication route to electronic devices, with FET structures which require high resolution patterning being defined by soft contact lithography, while passive components and interconnects are written by lower resolution digital printing and deposition methods. Silicon test structures are fabricated in house on heavily n-doped wafers, using thermally grown CMOS grade silica as dielectric and metal source and drain electrodes patterned by lift-off. Using poly(3-hexylthiophene) (P3HT) as the semiconductor on such a device, careful processing allows us to achieve on/off current ratios up to 10ˆ8, corresponding to the measurement limit of our present equipment in Ioff. The field effect mobility observed is comparable with results previously reported for P3HT devices. Printed devices are based on soft contact lithographic patterning of a catalytic surface, followed by electroless metalisation. Use of this route allows us to fabricate devices routinely with channel lengths at least down to 2.5 microns, and achieve higher yields than with lift-off processed metal. A number of solution processed single layer and multilayer dielectrics have been tested; choice is determined by the dual compatibility requirements of metal and polymer deposition. The resulting devices show a number of artefacts compared to those fabricated on silicon, the majority of which can be traced to shortcomings in the dielectric layer. In particular the on/off current ratio is limited to about 10ˆ4 by significant leakage paths to the gate electrode, and an offset is imposed on the threshold voltage. Our work nevertheless demonstrates direct fabrication of working devices with useful performance onto substrates as unfavourable as standard display grade ITO glass. Prospects for improvement of the processing and device performance are assessed.

3:15 PM H4.4
Novel 3-D MEMS Approach to Digitally Printing Organic Semiconductors. Martin W. Schoeppler[2] and Linda T. Creagh[1];
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Ink jet printheads are now widely used in manufacturing processes that require precise dispensing of materials. Today, Spectra manufactures a variety of drop-on-demand ink jet printheads for the industrial printing market, but new markets present fresh challenges to our technology. In response to requirements for dispensing novel electronic fluids, we are developing next generation jetting technology based on our silicon MEMS technology with three-dimensional silicon technology and piezo-based pumping chambers integrated into the chip structure. This presentation will discuss the current status of ink jet printing as a manufacturing process in the electronics industry. It will address the functional and physical design features and properties of Spectra's MEMS process, its characteristics, reliability and usability. To meet the needs for a simple R&D tool, Spectra has designed a Lab Deposition System that couples disposable ink jet modules with a simple x,y-stage. The Lab Deposition System has the capability to visualize drops in flight, key to understanding the dynamic performance of unique fluids. Examples of opportunities and applications in electronics printing for MEMS-based ink jet technology will be presented.

3:30 PM H4.5
High-Mobility Ambipolar Field-Effect Transistors Based on Transition Metal Dichalcogenides. Vitaly Podzorov[1], R. Zeis[2], Christian Kloc[2], Ernst Bucher[2] and Michael Gershenson[1];
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We report on fabrication of a novel class of high mobility field-effect transistors based on transition metal dichalcogenides [1]. The unique structure of the single crystals of these layered inorganic semiconductors enables fabrication of FETs with intrinsically low field-effect threshold and high charge carrier mobility, comparable to that in the best single-crystal Si FETs (up to 500 cm2/Vs for the p-type conductivity in the WSe2-based FETs at room temperature). Among other interesting properties of these FETs are the ambipolar operation and mechanical flexibility. These remarkable characteristics make FETs based on transition metal dichalcogenides very attractive for basic research and for applications in "flexible" electronics. Supported by the NSF (DMR 0405208, ECE 0437932) and ARO MURI (DAAD 19-99-1-0252). [1] V. Podzorov et al., Appl. Phys. Lett. 84, 3301 (2004).

3:45 PM H4.6
Polyaniline Films on Flexible Substrates for Strain Gauge Applications. Rodrigo Fernando Bianchi[1], Enia Mara[1], Silmar A. Travain[3], Fernando Josepetti Fonseca[1], Ely Antonio Tadeu Dirani[1,2] and Adnei Melges de Andrade[1];
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This work describes the design and the operation of thin polyaniline films used to produce a conducting polymer base-strain gauge sensor. Polymer strain gauges are of great interest due to their large recoverable strains, low cost, and potential for integration with other polymer devices, including diodes, transistors and batteries. Thin polyaniline films were prepared by in-situ polymerization method on an interdigitated chromium-gold microelectrodes previously deposited on poly(ethylene teraphthalate) - PET substrates. The electrical characteristics of the polymer device were carried out as function of the polyaniline doping level using a Wheatstone bridge circuit in order to improve the device performance and efficiency. This circuitry allows the measurement of small strains characteristics of the polymer system deformation around 0.1 % and gauge factor higher than 5, which is typical of inorganic solids material under tension. The excellent adherence of the PANI films on PET, as well as the recoverable strain of greater than 1 % may be useful in the design of future devices. This work was sponsored by Fapesp, CNPq and IMMP/MCT.

4:00 PM *H4.7
Electrical Characterization of Transmission Lines on Non-Woven Textile Substrates. Troy Nagle, Carey Merritt, Tae-Ho Kang, Burcak Karaguzel, John Wilson, Edward Grant and Behnam Pourdeyhimi;
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This paper deals with the electrical characterization of coplanar waveguide (CPW) transmission lines printed onto non-woven textile substrates using conductive inks. After the transmission lines were printed, tests were carried out to determine their suitability for wide-band applications (e.g., digital signaling). The tests for the conductive-ink line characterizations included DC parameters and Time-Domain Reflectometry metrics. The transmission-line test samples were screen printed onto three different, carefully selected types of non-woven textile substrates using conductive inks of different compositions and viscosities. The printed test samples show visual variations in the continuity of the transmission lines, giving rise to geometrical variations in the CPW structure and characterization parameters. A custom test fixture was fabricated to allow the use of traditional microwave probing techniques during the characterization phase, and thus to reduce the errors derived from measurement interconnects. The methods described are scalable to large area flexible and stretchable textile substrates.