SYMPOSIUM B

Materials, Technology, and Reliability of Advanced Interconnects

March 28 - April 1, 2005

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* Invited paper

TUTORIAL

Wafer Level Packaging–Materials, Process, and Reliability
Monday March 28, 2005
1:00 PM - 5:00 PM
Room 2004 (Moscone West)

Wafer Level Packaging (WLP) has gained momentum in the small chip arena, driven by needs for cost reduction, form-factor shrinkage, and enhanced performance. Advantages in performing burn-in and test at the wafer level will lower the IC cost and resolve the known good die (KGD) issues that are concerns to the electronic industry. WLP will merge the front-end IC fabrication with the back-end discrete packaging, and provide a paradigm shift in the electronic packaging industry. This course will provide an overview of the recent advances on WLP, the advantages and challenges in terms of materials (conventional polymers as well as nano functional materials), processes (with ultra fine pitch flip chip interconnects), and reliability in these new packaging technologies.

COURSE OUTLINE

- Overview of Electronic Packaging: Present and Future Trends
- Definition of Wafer-Level Packaging
- Market Drivers for WLP
- Overview of Various WLP Configurations and Process Techniques in the Industry
- Barriers and Challenges with WLP Technologies
- Fundamentals of Polymers and their Physical and Mechanical Properties and Measurements
- Overview of Inorganic and Organic Polymers for Electronic Packaging
  - Silicon Dioxides, Nitrides & Oxynitrides
  - Epoxies, Silicones, Polyimides, Silicone-Polyimides, Polyurethanes
  - Benzocyclobutenes, Parylenes, BT Resins, Sycars, Polyesters, High Temperature & Liquid-Crystal Polymers, Low-k, Low Loss and Nanofunctional and Foam Materials
- Recent Advances on Low Cost Flip Chip: Materials, Processes and Reliability
- Lead-free Interconnect Alternative Materials- Electrically Conductive Adhesives
- Next Generation WLPs

This tutorial will be of interest to engineers, scientists, and managers involved in the design, process, and manufacturing of IC electronic components, modules, and hybrid packaging, as well as electronic materials suppliers involved in materials manufacturing and research & development.

Instructors:
C. P. Wong, Georgia Institute of Technology
Luu Nguyen, National Semiconductor Corp.

SESSION B1: Characterization of Low-K Dielectrics
Chairs: Andrew McKerrow and Todd Ryan
Tuesday Morning, March 29, 2005
Room 2004 (Moscone West)

8:30 AM *B1.1
Fracture and Mechanical Behavior in Thin-Film Interconnect Structures: Challenges for Next Technology Nodes.
Reinhold Dauskardt, Department of Materials Science and Engineering, Stanford University, Stanford, California.

Delamination of interfaces and cohesive cracking of fragile interlayer dielectrics effects the mechanical integrity of thin-film interconnect device structures. This results in reduced yield at all levels of device processing including survival through chemical mechanical planarization (CMP) and subsequent device packaging. Unique challenges for next technology nodes involve the introduction of low and ultra-low k dielectric materials, smooth and non-stoichiometic interfaces from atomic layer deposition, and the effect of interconnect architecture including length-scales, aspect ratios, and metal density. These problems are compounded by the generic problem of packaging fragile interconnect structures. Materials and interfaces are nearly always optimized for other desired properties (e.g. dielectric properties or diffusion resistance) and the resulting effects on mechanical performance can be significant. In this presentation, the mechanical and fracture behavior of representative blanket and patterned thin-film structures including dielectrics, barriers, metal and underfill layers are examined. The acceleration of crack growth in complex chemical environments and under thermomechanical loading typically encountered during processing is discussed. The effects of interface parameters and material composition and porosity will also be considered. Novel strategies to toughen fragile materials and interfaces are described. Finally, the effect of more complex patterned thin-film structures are examined where length scales are restricted in more than one dimension. Implications for device reliability, integration of new materials, and life prediction are discussed.

9:00 AM B1.2
A New Technique for the Characterization of the Adhesion in Patterned Films. Ibon Ocana[1], Jon Molina[1], Diego Gonzalez[1], M. Reyes Elizalde[1], J. Manuel Sanchez[1], J. Manuel Martinez-Esnaola[1], Javier Gil-Sevillano[1], Tracey Scherban[2], Daniel Pantuso[2], Brad Sun[2], Jessica Xu[2], Barbara Miner[2], Jun He[2] and Jose A. Maiz[2]; [1]CEIT (Centro de Estudios e Investigaciones Tecnicas de Gipuzkoa) and TECNUN (University of Navarra), San Sebastian, Gipuzkoa, Spain; [2]Intel Corporation, Hillsboro, Oregon.

The thermo-mechanical robustness of interconnect structures is a key reliability concern for integrated circuits. The miniaturization process and the package/silicon interaction result in an increase of the thermal stresses whilst the use of new low-k materials, with degraded mechanical properties, makes it more and more difficult to predict their in-service behavior. Cross-sectional nanoindentation (CSN) has been successfully used so far to characterize interfacial adhesion in blanket thin films. In this paper, a modification of this technique is introduced to characterize adhesion and crack propagation in interconnect structures. The new technique is called modified cross-sectional nanoindentation (MCSN) and, as in conventional CSN, a Berkovich indenter is used to initiate fracture in the silicon substrate near the interconnect structure. The cracks propagate through this structure, preferentially along the weakest interfaces in the system. In this novel technique, an FIB (Focused Ion Beam) workstation is used for sample preparation, to machine a trench parallel to the indented surface. In this way, crack growth can be better controlled, and the process may be modeled in two dimensions. The technique has been applied to test chips simulating interconnect structures, with different types of etch-stop (ES) films and different metal densities. The results obtained using this technique correlate well with the interfacial adhesion measured by four-point bending (4 PB) in blanket films. The MCSN technique proposed in this paper is better suited to study local adhesion in patterned structures and has also proven useful for the study of crack propagation through the interconnect structure, making it possible to assess the effect of metal density in the overall behavior of the crack. FE modeling of the stress fields in the immediate vicinity of the crack tip has been carried out to understand the crack paths observed.

9:15 AM *B1.3
Mechanics of Advanced Interconnect Structures. Zhigang Suo, Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

This talk draws on recent experiments and theories concerning the mechanics of integrated structures (Jun He and Z. Suo, Statistics of electromigration lifetime analyzed using a deterministic transient model; Jun He, Guanghai Xu, Z. Suo, Experimental determination of crack driving forces in integrated structures. Preprints are available online: www.deas.harvard.edu/suo, publication 163 and 164). The interconnect structures on the microprocessor chips are undergoing significant changes in recent years. In particular, a family of low-permittivity dielectrics, the organosilicate glasses (OSGs), have been integrated into the interconnect structures. The OSGs have low toughness and low elastic modulus, so that the interconnects are susceptible to cracking and electromigration damage. In principle, the crack driving force G can be calculated by solving an elasticity boundary value problem. In practice, however, such a calculation is prohibitively difficult for integrated structures of complex architectures, diverse materials and small features. On the other hand, it costs little to make many replicates of an integrated structure, so that massive testing is affordable. We describe an experimental method to measure G. We will also describe a new approach to analyze electromigration.

9:45 AM B1.4
Mechanical Properties of Porous MSQ Films: Impact of the Porogen Loading and Matrix Crosslinking. Frederic Ciaramella[1], Vincent Jousseaume[1], Sylvain Maitrejean[1], Bruno Remiat[1], Marc Verdier[2], Maurine Montagnat[2] and Gerard Passemard[3]; [1]CEA-LETI, Grenoble, France; [2]LTPCM, Grenoble, France; [3]STMicroelectronics, Grenoble, France.

Semiconductor industry needs a continuously improvement of integrated circuits performance and an increase of integrated density on silicon. The 2003 ITRS Roadmap underlines the need of dielectric material for ILD with dielectric constant (k) lower than 3 for the 90 nm node and than 2.4 for the 45 nm node. In this work, porous film with k value lower than 2.2 were deposited using a methylsilsesquioxane (MSQ) as matrix and organic nanoparticles as porogen. After deposition and baking, this composite was thermally cured to allow the porogens degradation and matrix crosslinking and then form the porous structure. Different k values were obtained by varying the porogen loading in the composite. In this work, the mechanical properties of the composite and the porous films (before and after porogen removal respectively) were investigated using nanoindentation analysis and FTIR for different porogen loading (between 0 % and 40 %). It is shown that the composite modulus is higher than the porous film modulus for high porogen loading. The evolution of hardness versus porogen loading underlines that the porous films mechanical properties are better than dense one for each porogen loading due to a better matrix crosslinking. The mechanical properties were modelized using foam mechanical models [1]. Different configurations were investigated to simulate the film structure (cubic or tetrakaidecaedric cells, open or closed porosity, compression or flexion stress). For the porous film, the hardness analyses underline that a good model agreement is obtained with closed cells for the low porosity film and with open cells for high porosity samples. The best Young modulus fitting is obtained with tetrakaidecaedric cells. This seems in good agreement with porosity morphology. Finally, detailed FTIR measurements were performed in order to obtained precise informations of the matrix crosslinking. These analysis allows to propose a correlation between the matrix crosslinking and the mechanical properties of porous MSQ. [1] L.J. Gibson and M.F. Ashby, "Cellular Solids", Cambridge University Press, Cambridge, UK (1997)

10:30 AM B1.5
High-temperature Nanoindentation Measurement for Hardness and Modulus Evaluation of Low-k Films. Jiping Ye[1], Nobuo Kojima[1], Satoshi Shimizu[1] and James M. Burkstrand[2]; [1]Research Dept., Nissan ARC Ltd., Yokosuka, Japan; [2]Hysitron, Inc., Minneapolis, Minnesota.

Low-k dielectrics have attracted widespread interest for use as inter-metal dielectric materials to reduce interconnect resistance in ultra-large-scale integrated devices. Integration processes and practical use environments require low-k dielectric materials not only to possess a low, stable and isotropic dielectric constant, but also to have thermal and mechanical stability at high temperature as well as low moisture absorption. As a technique for estimating mechanical properties, nanoindentation measurement has been widely used to evaluate the hardness and modulus of low-k films. This measurement method applies an indentation load in the micro newton range by pressing a diamond stylus on the specimen surface and then detects the penetration depth on a nanometer scale. The rigorous accuracy required for loading and displacing the stylus has made it difficult to apply nanoindentation measurement at high temperature. Up to now nanoindentation measurement for evaluating the mechanical properties of thin films has been restricted to room temperature (RT). In this work, an attempt was made to apply nanoindentation measurement at high temperatures up to 200°C for evaluating the temperature dependence of the hardness and modulus of low-k films. A foam insulator plate and a water-cooling system were incorporated in a Hysitron nanoindentation system to protect the transducer, used for loading and detecting the displacement of the stylus, against heat convection from the heating stage. To reduce thermal load drift and noise further, a macor insulating holder was used to prevent heat conduction from the diamond stylus to the transducer. Measurement reliability was examined by using a thermomechanically stable SiO_2 film and an unstable organic low-k film of the same 500-nm thickness grown on a Si wafer. The SiO_2 film exhibited no significant change in hardness and modulus from RT to 200°C. This indicated that no thermal load drift and noise affected the measurement even at temperatures up to that level. In contrast, the hardness and modulus of the organic low-k film significantly decreased as the heating temperature was raised from RT to 200°C, although this low-k film showed good heat resistance, maintaining a stable temperature up to 450°C. It is thought that this reduction in mechanical properties originated from thermal stress relief and moisture desorption that occurred at the onset of specimen heating. The results of this study indicate that a high-temperature nanoindentation measurement method has been successfully developed for use in evaluating the mechanical properties of thin films and low-k materials at temperatures up to 200°C.

10:45 AM B1.6
Depth-profiling Pore Morphology in Nanoporous Thin Films Using Positronium Annihilation Lifetime Spectroscopy. Richard S. Vallery[1], Hua-Gen Peng[1], William E. Frieze[1], David W. Gidley[1], Darren Moore[2] and Richard J. Carter[2]; [1]Physics, University of Michigan, Ann Arbor, Michigan; [2]LSI Logic Corporation, Gresham, Oregon.

The continuing improvement of the integrated circuit speed demands implementation of nanoporous low dielectric constant (low-k) interlayer dielectrics. Monitoring pore characteristics in sub-micron, amorphous films with 0.5-10 nm pores is challenging. Beam-based positronium annihilation lifetime spectroscopy (PALS) utilizes a low energy beam of positrons to control implantation depth, which enables the analysis of thin films. This unique, non-destructive technique can guide both the development and integration of low-k dielectrics. The pore morphology of a PECVD ultra-low-k (ULK) film of k=2.2 is revealed using beam-based PALS combined with etching. Depth-profiling this film with PALS demonstrates inhomogeneous pore size distribution with film depth. Detailed analysis indicates that the ULK film has a layered structure comprised of a dense sealing surface layer, followed by an intermediate layer embedded with 1.8 nm pores and a deep region with ~3 nm mesopores. The larger porogen-induced pores are determined to be highly interconnected by further PALS measurement on the etch-backed film. The inhomogeneous porous structure of this film is responsible for the bowing and void formation damage observed in this film after integration.

11:00 AM B1.7
Linear versus Star Shaped Porogen Effects on Thin Film Pore Structure: X-ray Porosimetry and Neutron Scattering Studies. Hae-Jeong Lee[1], Christopher L. Soles[1], Bryan D. Vogt[1], Da-Wei Liu[1], Wen-li Wu[1], Eric K. Lin[1], Ho-Cheol Kim[2], Victor Lee[2], Teddie Magbitang[2], Phillip Brock[2], Willi Volksen[2] and Robert D. Miller[2]; [1]Polymers Division, National Institute of Standards and Technology, Gaithersburg, Maryland; [2]IBM Research Division, Almaden Research Center, San Jose, California.

Nanoporous materials are needed in advanced applications such as ultra low dielectric constant (low-k) layers for next generation integrated circuit device, bio-separation devices, and catalysts. Each application may require different pore dimensions and morphologies to achieve optimal performance. For example, low-k materials require uniformly distributed and isolated (not interconnected) small pores, while bio-separation needs interconnected larger pores. Characterizing the pore structure in thin films remains a significant challenge. New methods are needed to evaluate process-structure-property correlation. Detailed information can be determined with x-ray porosimetry (XRP) and a combination of x-ray reflectivity (XR) and small angle neutron scattering (SANS). XRP utilizes capillary condensation of solvent molecules (probe molecules) inside the accessible pores as a function of relative partial pressures, which could be converted into pore sizes using relationships such as the Kelvin equation. SANS is a complementary methodology to compare the structural information extracted from XRP. In this work, we studied influence of molecular architecture on the pore structures using two sets of porous samples, one for low-k application and one for bio-separation through a well-known porogen removal process. A thermally labile linear polymer (NG) and star shaped polymer (TP) are used as porogen materials for preparing porous low-k and bio-separation thin films, respectively. The effects of porogen type and loading (20 % and 50%) on the porous structure including pore size distribution (PSD), wall density, average density, average pore size, and pore connectivity are investigated. Samples with the same porogen loading contents show similar film densities regardless of porogen type. All the samples have approximately 10 % inherent micro pores in the wall material. TP samples have more obvious adsorption/desorption hysteresis loop in the XRP isotherms, suggesting that pores in those samples are more interconnected. In addition, adsorption and desorption of TP samples occur at narrow ranges of partial pressure, while NG samples display broad adsorption curves over a wide partial pressure range. These results indicate that TP samples have a narrow PSD. TP samples show prominent peaks in the SANS and SXR data, characteristic of ordered structures. The pore spacings are 140 Å and 158 Å for the 20 % and 50 % porogen loading samples, respectively. NG samples display relatively low scattering intensities, indicating smaller pore size. Average pore size of 20 % and 50 % NG samples are analyzed to be 17 Å and 80 Å in diameter, respectively.

11:15 AM B1.8
Solid State MAS NMR Spectroscopic Characterization of Plasma Damage and UV Modification of Low k Dielectric Films. Thomas Abell[1], Kristof Houthoofd[2], Francesca Iacopi[3], Piet

Grobet[2] and Karen Maex[3]; [1]Intel at IMEC, Leuven, Belgium; [2]Department of Agriculture, Katholic University Leuven, Leuven, Belgium; [3]IMEC, Leuven, Belgium.

Implementation of low k dielectric films has been delayed due to difficulties encountered in integration of the materials with standard patterning and processing techniques. One problem encountered has been the damage caused to the films by plasma-based patterning processes. Plasma damage leads to the increase of effective k-values and degradation of electrical reliability. Another problem encountered has been compatibility of low strength films with mechanically aggressive chemical mechanical polishing (CMP) and packaging processes. Post-deposition modification of the low k films has been pursued to increase the mechanical strength. UV curing has been recently demonstrated to increase the modulus and hardness with modest tradeoffs to electrical properties. Solid state 29Si and 13C magic angle spinning nuclear magnetic resonance (MAS NMR) spectroscopy is one promising technique for analysis of the atomic structure of low-k matrix materials. It was employed to characterize post-deposition modifications to the structure of low k dielectric films by plasma and UV treatments. Preparation of powders for NMR analysis from blanket depositions was performed for two different CVD deposited SiCOH films in the k~3.0 range. Tilted angle spinning (MAS), long recycle delay, large cycle numbers and high spinning rates were employed to improve the sensitivity and resolution of the spectra. Deconvolution of peaks in the spectra allowed relative quantification of local bonding states. Single thick depositions were compared to multiple layered depositions for investigation of plasma-related modification. UV curing of thick two-layer films was performed on one of the materials to investigate the structural changes which resulted in >40% increase in Young's modulus. NMR analysis was found capable of detecting changes in the short-range atomic structure due to plasma damage and UV cure treatments. Plasma induced damage registered in the 29Si spectra as an increase in Si-O crosslinking (Q groups) and a decrease in Si-OH groups (primarily Doh groups). This is consistent with other work showing densification of SiCOH surfaces into SiO2-like layers impermeable to organic solvents. Analysis of the 13C spectra was much more difficult due to poor sensitivity but changes were noted in signal intensity which may be due to plasma-related carbon depletion. Differences were also noted between the two dielectric materials in both 29Si and 13C spectra. UV curing also produced a shift in the spectra towards increased Si-O crosslinking (Q groups) and decreased Si-OH groups (Doh and Toh). Decreases were also observed in relative intensity of D and M groups. Changes in 13C spectra were noted with the appearance of a small peak in the spectra and a decrease in the signal intensity.

11:30 AM B1.9
Novel Electrical Metrology for Microcharacterization of Low-k Dielectrics. Vladimir V. Talanov, Robert L. Moreland, Andre Scherz, Bin Ming and Andrew R. Schwartz; Neocera, Inc., Beltsville, Maryland.

We will present a novel scanned probe technique for localized electrical metrology of low-k inter-layer dielectrics. The technique addresses two major challenges in characterization of advanced interconnects: product wafer compatible dielectric constant measurement on blanket films and stacks, and assessment of the extent of the dielectric damage caused by the integration of a low-k into a Damascene structure both before and after Cu metallization. The technique is based on a near-field microwave probe, the spatial resolution of which is defined by the probe geometry rather than by the wavelength of the radiation used. Therefore, even for microwave frequencies with wavelengths of centimeters our unique near-field probe can achieve spatial resolution down to a few microns scale. Using such a probe we are able to make product-wafer compatible quantitative measurements on both blanket low-k films and patterned structures. When the probe tip is placed in close proximity to the sample its fringe capacitance depends on the sample under test, the tip geometry, and the tip-sample separation. We employ a unique microwave resonator operating at 4 GHz to measure this capacitance with resolution down to 0.1 aF. The tip-sample distance is controlled by the modified shear-force technique. Extraction of the k-value for blanket film is based on an original theory, which provides for direct removal of the substrate contribution. The method is non-contact, requires no sample preparation, and can be used for both non-porous and porous films (including ultralow-k) and stacks with or without a capping layer. Because of the few-micron probing area the measurement could be performed over a test region in the scribe line. The technique is capable of measuring the blanket film k-value with a precision better than 0.5% and long term repeatability better than 1%. Because of the very high capacitance sensitivity the technique can also be applied to measure the effective dielectric constant of etched low-k structures prior to metallization as well as the line-to-line capacitance on small metallized test structures with area on the order of 10x20 micron. We will demonstrate blanket film measurements on a variety of low-k materials and show excellent correlation with mercury probe, as well as wafer mapping capability. In addition, the measurements on etched dielectric trenches as well as capacitance test structures will be presented.

SESSION B2: Low-K Dielectrics: Integration Issues
Chairs: Reinhold Dauskardt and Francesca Iacopi
Tuesday Afternoon, March 29, 2005
Room 2004 (Moscone West)

1:30 PM *B2.1
Nanoporous Materials Integration into Advanced Microprocessors. E. Todd Ryan[1], Cathy Labelle[1], Nicholas C. M. Fuller[2], Satya V. Nitta[2], Griselda Bonilla[2], Kenneth McCullough[2], Charles Taft[2], Hong Lin[2], Bum Ki Moon[3], Andrew Simon[2], Eva Simonyi[2], Mary Zaitz[2], Kelly Malone[2], Muthumanickam Sankarapandian[2], Zijian Li[4], Shuang Li[4], Yushan Yan[4], Junjun Liu[5] and Paul S. Ho[5]; [1]Advanced Micro Devices, Hopewell Junction, New York; [2]IBM Microelectronics, Semiconductor Research and Development Center, Hopewell Junction, New York; [3]Infineon Technologies, Hopewell Junction, New York; [4]Department of Chemical Engineering, University of California, Riverside, California; [5]Laboratory for Interconnect and Packaging, University of Texas, Austin, Texas.

Nanoporous low-k materials are critical for advancing microprocessor performance along the path of Moore's Law. Today, resistance-capacitance (RC) delay in back-end-of-line (BEoL) interconnects can limit microprocessor operation, necessitating improvements in both transistor and interconnect performance. BEoL performance enhancement has motivated the industry's transition from Al to Cu interconnects, and it also drives the integration of dielectric materials with lower dielectric constant (k-value). For decades, silicon dioxide (which has a k-value of ~4.0 - 4.2) was the insulator of choice. Fluorine-doped oxide was then introduced to lower the k-value to ~3.7, but adhesion and corrosion limited the F doping and k-value reduction. Carbon-doped oxides (or organosilicate glass, OSG) allow for greater C doping and k-values as low as ~2.6. OSG materials with k ~3.0 are in production now or will be soon, but future technologies are demanding even lower k-values. Further reducing the k-value of OSG materials requires the introduction of air into the film in the form of nanopores, but the introduction of pores creates many integration challenges. This talk will focus on some of the key challenges of using nanoporous materials as dielectric insulators in advanced microprocessors. These challenges include 1) controlling etch profiles, 2) difficulties in integrating nanoporous films due to their low mechanical strength, 3) difficulties in depositing a continuous metal layer onto a nanoporous surface, and 4) the susceptibility of nanoporous materials to damage by reactive plasmas used during microfabrication and methods to repair this damage. The talk will review research into controlling trench bottom roughness induced by etching and its relationship to pore size, maximizing mechanical strength by engineering optimal pore structures, sealing nanoporous surfaces, and repairing plasma damage using silylation chemistry.

2:00 PM B2.2
The Interaction of Hydrogen Plasmas with Ultralow-k Porous pSiCOH Dielectrics. Alfred Grill, Victoria Sternhagen and Vishnubhai Patel; IBM - T.J. Watson Research Center., Yorktown Heights, New York.

Hydrogen containing plasmas are being used to replace damaging oxidizing plasma for resist ashing in the integration of low to ultralow-k SiCOH dielectrics in the interconnect structures of ULSI devices. While the reducing hydrogen plasmas are less damaging to the SiCOH material than the oxidizing plasmas, they interact nevertheless with the dielectric and modify its characteristic. The current work investigated the interactions of hydrogen plasmas with ultralow-k porous SiCOH (pSiCOH) films and the dependency of these interactions on the values of the dielectric constant and on the porogen used for the preparation of the pSiCOH films. The effect of the substrate temperature has also been investigated. pSiCOH films of similar dielectric constants have been prepared by plasma-enhanced chemical vapor deposition (PECVD) using the same SiCOH precursor but two different organic porogens. The films exposed to the hydrogen plasmas have been characterized by optical techniques (FTIR spectroscopy and n&k measurements), shrinkage characterization, and electrical measurements on MIS structures. It was found that the hydrogen plasma modifies the structure of pSiCOH's oxide skeleton and reduces the concentration of the Si-CH3 bonds, resulting in an increase of the dielectric constant. The degree of modification, for films prepared from same precursors, is larger for films with lower dielectric constants (k) and is affected by the porogen used to prepare films with similar k values.

2:15 PM B2.3
Double-layered Structure of Surface Modification of Low-k Dielectrics Induced by He Plasma. Ken-ichi Yanai, Tadayoshi Hasebe, Kouji Sumiya, Seiki Oguni and Kazuhiro Koga; Consortium for Advanced Semiconductor Materials and Related Technologies, Kokubunji-shi, Tokyo, Japan.

Helium (He) plasma treatment of low-k dielectrics is usually used in Cu/low-k interconnect integration to improve adhesion to the cap SiO2 layer. To control this treatment precisely without degrading the dielectric layer, a fundamental understanding of surface modification induced by He plasma is essential. Thus, the changes in chemical bonds and atomic composition of the modification layer induced with different He plasma powers were investigated using infrared spectroscopy (IR) and X-ray photoelectron spectroscopy (XPS) at different take-off angles, 90° and 10°. The differential IR spectrum, measured at the SiOC film treated with He plasma, compared to the reference of that without the plasma treatment, exhibits a decrease in the absorbance of the peaks at 1273, 841, 800, and 774 cm-1, which arise from the Si-CH3 bond, and an increase in the absorbance of the peaks at 892 and 992 cm-1, which arise from the H-Si-O bond. With increasing He plasma power, the peaks of the Si-CH3 bond decrease and those of the H-Si-O bond increase monotonically. The decrease in the absorbance of the Si-CH3 bond of the SiOC film irradiated by He plasma at 300 W is about 17% of the total absorbance of the initial SiOC film when it is 92 nm thick. The surface modification layer is etched away with the mixed HF solution, whereas the SiOC film is not etched. The thickness of the modification layer, estimated from the etch depth, is 17 - 18 nm in the case of the He plasma at 300 W. In consideration of the decrease of the absorbance of the Si-CH3 bond evaluated from IR, almost all of the Si-CH3 bonds in the modification layer are broken using the He plasma. The etching behavior at the beginning of the treatment changes largely with the plasma power. Etching starts after some time interval in the case of the samples irradiated at over 300 W, whereas etching starts immediately in the case of irradiation at 100 W. This suggests that some further modification on the top surface takes place with the irradiation over 300 W. The atomic ratio of O/Si estimated from XPS spectra increases with He plasma treatment, resulting in a SiO2-like composition. The atomic ratio of C/Si decreases with the irradiation by He plasma at 100 W, indicating that some carbon atoms, which originate from the broken Si-CH3 bond, are sputtered away from the film. In the case of the irradiation at 300 W, the respective ratios of C/Si, estimated from the spectra at the take-off angles of 90° and 10°, are almost the same as or larger than that of the film without He plasma, indicating the depth profile is not homogeneous. In consideration of the escape depth of the photoelectron at each take-off angle, the top surface to be less than 1 nm of the modification layer changes to a carbon-rich composition, causing a double-layered structure in the modification layer. This work was supported by NEDO.

2:30 PM B2.4
Nanoscale Observation of Dielectric Damage to Low k MSQ Interconnects from Reactive Ion Etching and Ash Treatment. Todd S. Gross[1], Shaoning Yao[1] and Sri Satyanarayana[2]; [1]Mechanical Engineering, University of New Hampshire, Durham, New Hampshire; [2]SEMATECH, Austin, Texas.

Electrostatic force microscopy (EFM) was used to measure the extent of dielectric damage from plasma processing of nanoporous, low k methyl silsesqioxane (MSQ) interconnect structures with approximately 50 nm spatial resolution. Single level patterns were formed in 200 nm thick MSQ films by reactive ion etching (RIE) and were subsequently backfilled with an MSQ layer that was not exposed to plasma to act as a reference. The backfill was performed on as-etched structures with the photoresist intact and on structures in which the photoresist was removed by an oxygen plasma (ash) treatment. The EFM images on cross sections and feather sections show that the damage from the RIE penetrated ~100 nm in from the sidewall and that the redeposited polymer had a higher k than the MSQ (k~2.2). The ash treatment damaged the MSQ everywhere. Experiments are underway to determine if the ash damage results from diffusion of atomic oxygen through the nanoporous network or through the SiC hardmask.

2:45 PM B2.5
Surface Pore-Sealing in Porous MSQ Low-k Film using NH3 Plasma Treatment. Weide Wang[1], Dongzhi Chi[1], Jun Liu[1], Lei Wang[1], Soojin Chua[1], David W. Gidley[2] and Albert F. Yee[3]; [1]Institute of Materials Research & Engineering, Singapore, Singapore; [2]Department of Physics, University of Michigan, Ann Arbor, Michigan; [3]Department of Chemical Engineering & Materials Science, University of California, Irvine, California.

Films with interconnected mesopores pose a serious challenge for the integration of porous low-k dielectric films into the low-k/Cu interconnect scheme due to the difficulty of forming a thin, effective Cu diffusion barriers (e.g., Ta) on the sidewalls of vias/trenches. To maintain the integrity of the thin diffusion barrier, the pores on the sidewalls of the vias and trenches must be sealed before barrier deposition. In this paper, we report the formation of a thin, non-porous surface layer on a porous methyl-silsesquioxane (MSQ)-based dielectric film by NH3 plasma treatment. The porous MSQ films used in this study are Shipley's Zirkon 2200 low-k (k=2.2) films (about 1 mm thick). Depth profiling using beam-PALS (positronium annihilation lifetime spectroscopy) characterization showed that the pores in these films have an average diameter of 2.7 nm but with a much longer (~300 nm) pore interconnection length that allows a high fraction of the positronium (Ps) to diffuse into vacuum through the porous network. For the surface modification of the film, a low frequency (50.0 Hz-400.0 kHz) NH3 plasma treatment was carried out. The formation of a thin non-porous surface layer by NH3 plasma treatment was deduced based on the observations of (1) the curtailment of Ps diffusion into vacuum at every implantation energy and (2) an implantation-energy-independent Ps with the value also matching well with that of Ps formed in the non-plasma treated films with a 100 nm Si capping layer. From the SIMS depth profiling, it was found that the surface region is C-depleted, but with N incorporation, after NH3 plasma treatment. Cross-sectional TEM clearly showed the presence of modified surface layer with the thickness almost equal to that of C-depleted layer. It is believed that the C-depleted layer is indeed non-porous in nature, thus preventing the escape of Ps from the film into vacuum. With optimized processing parameters, e.g., 300 oC substrate temperature and 10 s plasma time, a very thin skin layer (~10 nm) can be formed without causing noticeable damage to the bulk of the low-k film (confirmed by FTIR). Substantial performance improvement was observed in the thin Ta barriers formed on the plasma induced non-porous skin layers.

3:30 PM B2.6
First Pass Study of Surface Modified Porous Low-k by Ion Implantation for Zero Thickness Barrier Requirement of Cu/MSQ/Si Stacks in Copper Metallization Scheme. Alok Nandini U. Roy, Zubin P. Patel and H. Bakhru; Physics, SUNY, Albany, Albany, New York.

Thin films of Ultra-Low k materials such as porous MSQ (k=2.2) were implanted with argon 1 x 1016 cm-2 dose at energies varying from 20 to 50 keV at room temperature. In this work we showed that the surface hardness of the porous films can be improved five times as compared to the as-deposited porous films by implanting Ar with 1 x 1016 cm-2 doses at 20 keV, sacrificing only a slight increase (~ 9%) in dielectric constant (e.g., from 2.2 to 2.4). The hardness persists after 450 0C annealing. The ion implantation process suppressed the moisture uptake in the porous low k films. Surface chemical modification made the films hydrophobic. In this paper, ion implantation strategy was pursued to create a SiO2-like surface on MSQ. The effects of implantation parameters on the barrier property and bulk stability of MSQ were then studied. The results reveal one possible route to attain the zero barrier thickness requirement for interconnects systems.

3:45 PM B2.7
Observation of Intrusion Rates of Hexamethyldisilazane during Supercritical Carbon Dioxide Functionalization of Triethoxyfluorosilane. P. M. Capani[1], B. P. Gorman[1], R. F. Reidy[1], D. W. Mueller[2,1], E. R. Walter[2], P. D. Matz[3], J. T. Rhoad[4] and E. L. Busch[4]; [1]Materials Science and Engineering, University of North Texas, Denton, Texas; [2]Physics, University of North Texas, Denton, Texas; [3]Silicon Technology Development, Texas Instruments, Inc, Dallas, Texas; [4]SEMATECH, Austin, Texas.

Water adsorption by porous low-κ silica films results in increased dielectric constants and is often due to silanol groups on the pore surfaces. Reacting the silanols with silylating agents (e.g., hexamethyldisilazane (HMDS) and trimethylchlorosilane (TMCS)) in supercritical CO_2 (SC-CO_2) can increase film hydrophobicity and can remove absorbed water. The SC-CO_2 has some solubility for the absorbed water and enhances the water removal process. Porous MSQ low-κ films often exhibit extensive loss of carbon species after plasma etch/ash processes, and supercritical silylation has demonstrated water removal and concomitant dielectric repair. Work by this and other groups have shown that the silylating agents do not deeply penetrate into the porous MSQ structure. To determine the impact of pore and penetrant size on supercritical silylation depth and diffusion rates, we have reacted porous low-κ's with a range of pores sizes and silylating agents with a range of sizes. Triethoxyfluorosilane (TEFS)-based xerogel films demonstrate enhanced mechanical properties (i.e., E=12GPa) and low dielectric constants (k=2.3) and can be synthesized with a range of pore sizes. Unlike MSQ, TEFS has no native methyl groups and, consequently, is hydrophilic. The absence of insipient carbon species in TEFS permits effective monitoring of silylation reactions through IR adsorption intensities of

S-CH_3 (1275cm^{-1}) and C-H (2980 cm^{-1}) because all carbon related IR adsorptions result from silylation. To observe these changes as a function of time, TEFS films have been treated with SC-CO_2 / HMDS (and other silylating agents) at different temperatures and pressures in an in-situ (supercritical) Fourier transform infrared (FTIR) spectroscopy cell. After supercritical silylation, the TEFS films have been characterized by contact angle measurements to note improvements to film hydrophobicity, capacitance-voltage (C-V) measurements to determine dielectric constants, ellipsometry to study changes in film porosity, and dynamic secondary ion mass spectrometry (DSIMS) and x-ray photoelectron spectroscopy (XPS) to chemically characterize the films as a function of depth.

4:00 PM B2.8

Supercritical Pore Sealing of Low-κ Films. P. K. Nerusu[1], R. F. Reidy[1], D. W. Mueller[2,1], P. M. Capani[1], P. D. Matz[4], E. L. Busch[3] and J. T. Rhoad[3]; [1]Materials Science and Engineering, University of North Texas, Denton, Texas; [2]Physics, University of North Texas, Denton, Texas; [3]SEMATECH, Austin, Texas; [4]Silicon Technology Development, Texas Instruments, Inc., Dallas, Texas.

To integrate porous low-κ films into the 45 nm technology node, metal intrusion into film pores must be prevented because it diminishes the insulating properties of the film by increasing its conductivity. Metal species penetration into porous films can be prevented by reacting film surface silanols with silylating solutes in a supercritical CO_2(SC-CO_2) solvent. It has been shown by our and other research groups that SC-CO_2 provides effective transport of bulky organic groups into low κ pore surfaces. In this study, a series of heat and chemical treatments were performed to observe the effectiveness of several SC-CO_2-based silylation agents as function of processing temperatures. The samples were heated to 400°C to condense adjacent or vicinal silanol groups into bridged oxygen species. C-V measurements were conducted to observe the change in κ with respect to temperature. The samples were then treated with a series of silylating agents (R_3-Si-Cl) with R=CH_3, C_2H_5, C_3H_7, C_4H_9, and C_6H_5, to observe their relative abilities to react with the remaining surface hydroxyls. Surface coverage of the silylating agents was examined using contact angle and X-ray photoelectron spectroscopy (XPS) measurements. In addition, contact angle experiments revealed that the hydrophobicity was diminished by heating the films to 400°C due in part to the loss of available reaction sites. Tetrakis (dimethyl amido) titanium (TDMAT) (diameter 1 nm), a TiN CVD precursor, was used to assess the ability of heat treatments and silylation to seal the pores. Cross-sectional scanning electron microscopy (SEM) and dynamic secondary ion mass spectroscopty (DSIMS) were used to view TiN penetration into the pores and capacitance-voltage (C-V) measurements were performed on the samples to calculate the change in κ value.

4:15 PM B2.9

The Deposition of Alkylmonochlorosilane Sealing Layers on Porous Methylsilsesquioxane Films Using Supercritical CO_2. Bo Xie and Anthony Muscat; Chemical & Environmental Engineering, University of Arizona, Tucson, Arizona.

Porous methylsilsesquioxane (p-MSQ) films (JSR LKD 5109) were treated with alkyldimethylmonochlorosilanes with alkyl chain lengths of one to eighteen carbon atoms dissolved in supercritical carbon dioxide to repair oxygen ashing damage and seal the pores in the film. Monochlorosilane concentrations in the range 78-103 ppm were delivered using supercritical CO2 at 150-300 atm and 50-60°C for a 2 min soak. Fourier transform infrared (FTIR) spectroscopy showed that trimethylchlorosilane (TMCS), butyldimethylchlorosilane (BDMCS), octyldimethylchlorosilane (ODMCS), decyldimethylchlorosilane (DDMCS) and octadecyldimethylchlorosilane (ODDMCS) reacted with both lone (SiO-H) silanol and H-bonded (SiO-H) silanol groups on the surfaces of the pores producing covalent Si-O-Si bonds with the surface. The FTIR also indicated that self-condensation of alkylsilanols produced a liquid film on the surface, which was partially removed using a pure $scCO_2$ rinse. There is a broad shoulder with a peak at 1116 cm-1 and a distinct shoulder at 1010 cm-1, which are indicative of a strained Si-O-Si bond formed by self-condensation of alkyldimethylmonochlorosilanes molecules (except for TMCS) and subsequent physisorption on the MSQ surface. The hydrophobicity of the blanket p-MSQ surface was recovered after silylation treatment as shown by contact angles >80°. The contact angle increased nearly linearly with the carbon chain length. The longer the carbon chain length, the higher the contact angle, which is consistent with literature results for monochlorosilanes (TMCS, ODMCS, and DDMCS) dissolved in liquid CO2 at 81.6 atm and 23° C for 24 hours [1]. CV measurements on metal-insulator-semiconductor capacitor devices made using the blanket films showed that the initial dielectric constant of 2.4 ± 0.1 increased to 3.5 ± 0.1 after oxygen plasma ashing [2] and was reduced to 2.42, 2.39, 2.42, 2.37, and 2.54 for TMCS, BDMCS, ODMCS, DDMCS, and ODDMCS treatments, respectively. Control of the penetration depth of silylation, thickness of the physisorbed layer, and film electrical properties will be necessary in order to use this approach to seal pores in MSQ films. There was no evidence for unreacted precursor or chlorine on the surface after processing with supercritical CO2 to the detection limits of FTIR, XPS, and Auger electron spectroscopy. Preliminary RBS measurements showed that copper diffused into untreated cured and ashed methylsilsesquioxane films but was prevented from diffusing by treatment with the eight-carbon alkylmonochlorosilane (ODMCS) and supercritical CO2. The cross-sectional SEM image shows that there was no copper penetration into the treated p-MSQ film, but that copper delaminated from the ODMCS treated surface as expected. Monochlorosilanes are candidate pore sealing additives. Reference: 1. C. Cao, A. Y. Fadeev, and T. J. McCarthy, Langmuir, 12 757 (2001). 2. B. Xie and A. J. Muscat, Microelectronic Engineering, 76, 52 (2004).

4:30 PM B2.10

A Cross-linkable Poly(p-xylylene) Derivative to Protect Ultra-Low κ Dielectrics. Brad P Carrow[1], Jay J. Senkevich[1], Toh-Ming Lu[2], Timothy S. Cale[2], Yunqing Chen[2] and Hassaram Bakhru[3]; [1]Brewer Science Inc., Rolla, Missouri; [2]Department of Physics, Applied Physics, and Astronomy, Rensselaer Polytechnic Institute, Troy, New York; [3]Department of Physics, SUNY-Albany, Albany, New York.

The development of new chemical vapor deposited polymer films capable of thermal cross-linking is described. We have shown that several halogenated xylenes are capable of CVD polymerization to form α-brominated and α-chlorinated poly(p-xylylene). The prepolymers were isothermally annealed to induce 1,2-dehydrohalogenation forming unsaturated poly(p-xylyene). Analogous to the formation of poly(p-phenylene vinylene) (PPV) from $\alpha,\alpha\prime$-dihalo-p-xylene, these films can undergo two stoichiometric hydrogen halide eliminations to form first halogenated PPV and finally poly(p-phenylene ethynylene) (PPE). Full conversion of the halogenated prepolymers was inhibited by rigid semi-crystalline regions formed at temperatures above ~225 °C during post-deposition annealing. Conversion did not proceed past α-halo PPV at 200 °C, yet increased heating resulted in crystallization preventing hydrogen halide elimination even at favorable temperatures. Still, the aliphatic unsaturated groups formed are capable of thermally induced cross-linking to form network polymers. The result is a process that yields robust ultra-thin and conformal organic barrier layers. This material could be useful as a thin capping layer over ultra-low κ (ULK) dielectrics to protect from photoresist ashing and to reduce brittle behavior. In the absence of full conversion, cross-linking of the vinyl groups began at ~475 °C. As a result, the incorporation of aliphatic substituents onto the aryl backbone is desirable to promote amorphous morphology and should allow for full conversion of the films. The base κ for these polymers is ~2.6 if all halogen is withdrawn during annealing, however if an alkyl substituent is introduced the dielectric constant can be reduced considerably. Yet even without side chains these polymer films possess very high thermal stability, >450 °C, and a leakage current density ~0.195 nA/cm^2 at 0.5 MV/cm. Copper directly deposited on the low κ polymers described here shows no evidence of diffusion from bias temperature stress (BTS) measurements after annealing at 400 °C and stressing at 150 °C and 1.0 MV/cm for 60 min.

4:45 PM B2.11

Integration of a Polymer Etch Stop Layer in a Porous Low K MLM Structure. Gregory C. Smith[1], Neil Henis[1,4], Richard McGowan[1,4], Brian White[1,2], Matthias Kraatz[1,5], Sri Satyanarayana[1], Sharath Hosali[1], Youfan Liu[1,3] and Klaus Pfeifer[1]; [1]SEMATECH, Austin, Texas; [2]Advanced Micro Devices, Austin, Texas; [3]Intel Corporation, Phoenix, Arizona; [4]Freescale Semiconductor, Austin, Texas; [5]University of Texas, Austin, Texas.

Etch stop layers have been integrated into porous low K structures in order to assure a flat etch front, and to help smooth the metal / dielectric interface in dual damascene systems [1]. The etch stop layer is used to solve within-wafer uniformity problems and microloading. The etch stop layers commonly used are silicon nitrides or silicon carbides, sometimes with incorporated oxygen or nitrogen. These layers have dielectric constants which are generally greater than that of silicon dioxide, which creates the dilemma of balancing the added process stabilization of using an etch stop with the reduced dielectric constant benefit of not having one. The usefulness of a porous low K structure hinges on how much lower the effective dielectric constant is than a silicon dioxide structure, which is generally much easier to integrate. In this work, a two level metal system was built using an organic polymer as the metal 2 etch stop layer. The polymer's dielectric constant of 3.3 compares with that of silicon carbide which is around 5. This leads to the expectation of a lower effective dielectric constant. The low dielectric constant of the polymer etch stop better matches that of the porous low K dielectric, which is 2.2. Compatibility with cleaning chemistry, and interpenetration with the

porous low K layer were investigated. Electrical performance of the second level of metal was used to choose a dual damascene etch process, and the RC product of 130 nm serpent resistors with comb capacitors was compared with the RC product on wafers with silicon carbide etch stop layers. [1] Y. Furukawa, et. al., Proceedings of International Interconnect Technology Conference 2002, pp 45-47.

SESSION B3: Low-K Dielectrics: Process and Integration Issues
Chairs: Ting Tsui and Joost Vlassak
Wednesday Morning, March 30, 2005
Room 2004 (Moscone West)

8:30 AM B3.1
The Pore Structure and Integration Performance of a Porous CVD Ultra Low k Dielectric. Youfan Liu[1], Andreas Knorr[2], Wen-Li Wu[3], David Gidlui[4] and Bernd Kastenmeier[5]; [1]Intel Assignee at SEMATECH, Austin, Texas; [2]Infineon Assignee at SEMATECH, Austin, Texas; [3]NIST, Gaithergburg, Maryland; [4]University of Michigan, Ann Arbor, Michigan; [5]IBM Assignee at SEMATECH, Austin, Texas.

Low dielectric constant (k) materials are required for future generation integrated circuit technologies. The updated projection of k for 45 nm technology nodes and beyond would be less than 2.2. Introducing porosity and minimizing the atomic bond polarization in dielectric materials are common approaches to decrease the dielectric constant of the materials. However, creating porous structures could have significant impacts on its property and integration performance in multilevel interconnect systems. Therefore, understanding pore structures and their impacts on property and integration performance is essential for material and integration process development. This paper presents the evaluation results on a porous PECVD ultra low k dielectric material (k = 2.0). We have integrated the low k dielectric into a one level metal (copper) system and have evaluated the electrical characteristics and the integration performance during integration processing such as chemical mechanical planarization (CMP), plasma etch and ash. We have also conducted film structure studies and investigated the implication of the structure on integration performance. This SiCOH based porous PECVD material has a fairly uniform composition distribution through its film thickness but has a significant depth gradient in pore structure. There is no porous structure on the top layer and the average pore size gradually increases with depth. The top dense layer provides strong adhesion to cap layers of SiC and SiCN as there is no delamination of patterned Cu/low k structures during the integration CMP process. The larger/open pore structures at the lower parts of the trench sidewalls received severe damages such as voids and carbon depletion during plasma patterning, which result in an unexpected high product of comb capacitance and serpentine resistance and high k effective of the integrated structure. Alternative patterning process, sidewall pore sealing, and modifying pore structures would be required to minimize the sidewall damages.

8:45 AM B3.2
Ultra Low K Pecvd Porogen Approach: Matrix Precursor Comparison and Porogen Removal Treatment Study. Laurent Favennec[1], Vincent Jousseaume[2] and Vincent Rouessac[3]; [1]STMicroelectronics, Crolles, France; [2]CEA / Leti, Grenoble, France; [3]IEM, Montpellier, France.

The introduction of new dielectrics into silicon chip interconnection technology is marked by continuous revisions to meet the ITRS projection. Amorphous a-SiOC:H (K=2.9) deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) from silane-like precursors (with an oxidant) is now in scale up towards production. Using other precursors like siloxanes, K value can be reduced till to 2.5. However, sub-65nm technologies need K values below 2.5 but also an extendable material to further K values reduction. Introducing porosity is the main way to reduce the dielectric constant. This work reports results concerning a two steps PECVD porogen approach to perform Ultra Low K (K<2.5). Firstly a dual-phase thin film is deposited by PECVD using two advanced precursors: a siloxane one, to create a-SiOC:H based matrix, and an organic precursor, i.e. the porogen, to create the sacrificial phase. The goal of this first step is to obtain a hybrid material: a matrix containing organic inclusions. In a second step, the porogen is removed by a suitable curing to generate porosity. In this work, cyclic and non-cyclic siloxanes were evaluated to create the matrix. Thin films were then fully characterized to understand chemistry influence. It is shown that it is possible to deposit hybrid material with both precursors. The siloxane choice, cyclic or not, seems not to have an impact on the dielectric constant. But FTIR analysis indicates that it may be determinant for interactions inside hybrid material and cross-linking phenomenon. Process study and physical characterisations were performed to well control ratio of organic phase incorporation. To better understand the porogen removal mechanism, different cures were investigated. Thermal cures under different conditions (N2, N2 H2 atmosphere with or without O2; different thermal ramp) were compared to a thermally assisted UV cure. Curing post treatments were done on different hybrid films (different precursors and porogen ratio). Using FTIR spectra and mechanical characterizations, it is shown that the curing step is a critical point because it combines two different phenomena: porogen removal (pores creation) and material cross-linking. The K value can be tuned by varying the porogen ratio and dielectric constant lower than 2.3 are obtained. Nitrogen adsorption isotherms analysis and Grazed Incidence Small Angle Scattering allow to explain the K decrease after cure, showing the porosity in the film. This work clearly demonstrates the ability of achieving an ULK by a PECVD porogen approach using different precursors for the matrix and for the porogen sacrificial phase. It also permits a better material behaviour understanding during hybrid deposition and during the curing.

9:00 AM B3.3
Film Properties and Integration Performance of a Nano-Porous Carbon Doped Oxide. Lester D'Cruz, Sang Ahn, Yi Zheng, Josephine Chang, Nagarajan Rajagopalan, Thomas Nowak, Alex Demos, Girish Dixit, Derek Witty and Hichem M'Saad; Dielectric Systems and Modules, Applied Materials, Inc., Santa Clara, California.

The semiconductor industry has witnessed a successful introduction of copper based interconnects and low permittivity insulators with 130nm node devices. The advent of 90nm node devices with even lower permittivity insulators such as carbon doped dielectrics has resulted in increasingly complex integration challenges related to interfaces between the different dielectric layers, as well as between the dielectric and metal layers. Continued scaling poses even greater obstacles, requiring innovative films and integration techniques. Good mechanical properties for both the bulk low k dielectric and related dielectrics comprising the film stack remain essential to produce a stable integral multi-level metal structure. Carbon doped dielectrics used in 90nm node devices achieved k$\sim$3.0 through the lower polarizability of the Si-C bond compared to Si-O and the introduction of constitutive porosity enabled by the larger CHx groups in the oxide matrix. However, inter-level dielectric layers for the 65nm technology node and beyond require carbon-doped oxide (CDO) films with k<2.5. It has been shown that incorporation of nanometer-sized pores into CDO films can enable k values below 2.5. An emerging approach implements co-deposition of a CDO film and an organic compound using plasma enhanced chemical vapor deposition (PECVD). The process is optimized in a manner such that some of the organic material can be incorporated, and porosity is subsequently created by removing the thermally labile organic species using a post-treatment. While achieving low k through the nano-porous approach, it is critical to maintain the mechanical strength at a level that will ensure stable integration. Understanding the effects of film processing parameters on the evolution of porosity and the correlation of porosity with modulus and hardness is essential to the development of an ideal advanced low k dielectric film. This paper describes a k<2.5 porous CDO film deposited by PECVD that is resistant to moisture uptake and thermally stable during subsequent processing. The film is deposited in a conventional PECVD reactor and is treated after deposition using a patented cure technology. Film properties and integration results will be presented to show the viability of integrating this film into a conventional dual damascene interconnect flow.

9:15 AM B3.4
Determining Pore Structure and Growth Mechanisms in Templated Nanoporous Low-k Films. Hua-Gen Peng[1], Richard S. Vallery[1], Ming Liu[1], David W. Gidley[1] and Jin-Heong Yim[2]; [1]Physics, University of Michigan, Ann Arbor, Michigan; [2]Materials Lab, Samsung Advanced Institute of Technology (SAIT), Yongin-Si, Gyeonggi-Do, South Korea.

Templating is one of the most popular methods for generating nanocomposite and nanoporous films and the resultant pore size and pore interconnection length depend strongly on the combination of host matrix and porogen used. Positronium Annihilation Lifetime Spectroscopy (PALS) analysis has been performed on a range of films produced using several cyclodextrin (CD) and Calix-arene (CA) porogens in a modified MSQ host matrix. PALS reveals the role of functional groups on the CD's and CA's in determining the resulting pore structure, both size and interconnection length, versus porosity. In this systematic study, three distinct pore growth modes were observed depending on the porogen-porogen and porogen-matrix interactions. A CD-based porogen with trimethoxy-siloxyl functional groups (sCD) produces pores of constant diameter, but with interconnection length much longer than the pore diameter for all porosities. The functional groups of sCD are such that they should form Si-O-Si covalent bonds after hydrolysis into silanol groups, therefore linear chains of sCD molecules are readily polymerized,

producing longer interconnected pores of constant cross section. A second CD porogen with only methoxyl functional groups (tCD) has weaker Van der Waals interactions. The aggregation of the porogen domains is expected to be more 3-dimensional (pseudo-random), with isolated pores consistent with a template of the tCD molecular size at low porosity which then gradually increase in pore size and interconnection length as porosity increases. Computer simulations using a random pore growth and nucleation model show consistent trends for pore size growth. The CA system, being amphiphilic, acts like a surfactant and beyond some critical concentration should promote large micellar domain growth. Explosive pore growth between 7% and 15% porosity is detected by PALS. These results clearly demonstrate three different aggregation modes with porogen concentration for the resulting nanopores; from isolated molecules to interconnected network. It is a key demonstration of the usefulness of PALS in untangling the fundamental pore structure and its evolution in porosity. PALS characterization of porosity provides novel feedback in understanding and design of nanoporous materials.

9:30 AM B3.5
Nanometer-scale Pore Formation in a Polyphenylene Low-k Dielectric. Michael S. Silverstein[1], Barry J. Bauer[2], Ronald C. Hedden[2], Hae-Jeong Lee[2] and Brian G. Landes[3]; [1]Materials Engineering, Technion - Israel Institute of Technology, Haifa, Israel; [2]Polymers Division, National Institute of Standards and Technology, Gaithersburg, Maryland; [3]Dow Chemical Company, Midland, Michigan.

Nanometer-scale porosity is being introduced into low-k dielectrics in an attempt to achieve interlevel metal insulators with permittivities of less than 2.0. It has proven extremely difficult to describe pore formation and to characterize the porous structure. This work investigates pore formation in a low-k dielectric based on pyrolysis of a porogen (26 % by volume) in a polyphenylene matrix. One unique aspect of this research is the description of the nanoscale structure at various stages of pore formation through the use of a deuterated porogen. The combination of x-ray reflectivity (XRR) and small angle neutron scattering (SANS) was found to be a powerful technique for describing the changes in the materials during porogen degradation and pore formation. The average radius of the porogen domains was approximately 60 Å and the size distribution was relatively broad. The numerous smaller porogen domains collapse during degradation, while the larger domains tend to yield stable pores. The collapse produces a significant reduction in film thickness, a porosity that is significantly smaller than the porogen content, a pore size distribution that is narrower than the porogen domain size distribution and an average pore size of approximately 80 Å SANS porosimetry using a match point solvent and XRR porosimetry were used to provide more information regarding the pore size distribution.

10:15 AM *B3.6
Channel Cracking in Low-k Interconnect Structures. T. M. Shaw[1], Xiao Hu Liu[1], Michael Lane[1], Robert Rosenberg[1], Sarah L. Lane[2], James Doyle[1], Darryl Restaino[2], Steven Vogt[2] and Daniel Edelstein[1]; [1]IBM Research, Yorktown Heights, New York; [2]IBM Microelectronics, Hopewell Junction, New York.

The drive to reduce the dielectric constant of dielectrics for backend of the line structures has resulted in a corresponding reduction in their mechanical strength. As a result of this reduction in strength dielectric films have become more susceptible to channel cracking driven by tensile stresses in the films. Recent theoretical studies have suggested that the critical thickness for cracking can be substantially reduced by the presence of patterned structures under a blanket dielectric film. In particular narrow gaps between metal features are expected to greatly reduce the critical thickness for channel cracking. As such features are common in multilevel interconnect structures, it is important to quantitatively establish the conditions in which lead to channel cracking for specific interconnect geometries. We have used finite element analysis to examine the susceptibility of different geometries to channel cracking and shown that for realistic interconnect structures the crack driving force can be enhanced by more that an order of magnitude over that for a blanket film. Thickness and modulus of the dielectric underlayer as well the location and spacing of metal features all contribute to the enhancement. Based on the analysis we have built multilayer test structures exhibit the predicted enhancement. From measurements of crack velocities in a controlled environment we have been able to confirm the key features of the model. In particular we have shown that the behavior is quantitatively in agreement with an elastic model in which stresses arise from thermal expansion mismatch of the dielectric and the interconnect. Details of the analysis and experiments will be given in the talk and used to discuss the effects that grain structure and plasticity have on the crack driving force with different interconnect geometries.

10:45 AM B3.7
The Size Effect of Nanoparticular Porogen on the Mechanical Properties of Nanoporous Ultra-low Dielectric Materials. Sung-Kyu Min[1], Jae Jin Shin[1], Se Jung Park[1], Bongjin Moon[2], Do Young Yoon[3] and Hee-Woo Rhee[1]; [1]Department of Chemical & Biomolecular Engineering, Sogang University, Seoul, South Korea; [2]Department of Chemistry, Sogang University, Seoul, South Korea; [3]Department of Chemistry, Seoul University, Seoul, South Korea.

Although there are a lot of nanoporous low dielectric materials prepared by organosilicate matrix and sacrificial porogen, for example, star-shaped poly(caprolactone) and surfactants, they have been limited to use as interlayer dielectrics for the next generation semiconductor because the increase in the porosity seriously decreases the mechanical strengths of nanoporous low-k films such as elastic modulus and surface hardness. Therefore, it is important to minimize the decrease in the mechanical strengths upon the porosity by controlling pore morphologies like pore size and its size distribution. In this study, we used two different sizes of chemically reactive nanoparticular porogens based on the glucose unit. The porogens were functionalized through allylation and hydrosilylation reactions and the matrix used was poly(methyltrimethoxy silane-co-bistriethoxysilyl ethane) [poly(MTMS-co-BTESE)]. Even though the increase in the porosity led to decrease in the k value, triethoxysilyl glucose (TESGC) resulted in much higher mechanical strengths than triethoxysilyl b-cyclodextrin (TESCD) due to the smaller pore size.

11:00 AM B3.8
Fracture Property Improvements of a Nanoporous Thin Film Via Post Deposition Bond Modifications. Jeannette M. Jacques, Ting Y. Tsui, Andrew J. McKerrow and Robert Kraft; Silicon Technology Development, Texas Instruments, Inc., Dallas, Texas.

As silicon-based microelectronic devices continue to aggressively scale down in size, traditional BEOL dielectric materials have become obsolete due to their relatively high dielectric constant. For 90 nm node devices, the group of materials known as organosilicate glass (OSG) has emerged as the predominant choice for intermetal dielectrics. A potential failure mechanism for this class of low-k dielectric films during the manufacturing process is catastrophic fracture due to channel cracking. The driving force for channel cracking is dependent upon several film properties, including the modulus and residual tensile stress. The use of an electron beam curing process is being evaluated within the semiconductor industry as a mean for improving the mechanical strength of these silicon-based materials. Within this work, the effects of curing dose (micro-C/cm^2) upon the mechanical properties of OSG thin films were characterized. For a set process voltage and current, linear relationships exist between the dose and several mechanical film properties. However, at very high curing doses, a highly concentrated surface region forms, resulting in dramatically different film behavior. Channel crack growth velocities were also measured for these cured materials. As the cure dose is increased, the crack growth rate decreases according to a power law relationship. The structural film changes induced by the electron beam cure process are addressed, focusing on their impact upon the mechanical strength of OSG thin films.

11:15 AM B3.9
Effects of UV-Cure on Mechanical, Physical and Electrical Properties of Microporous SiOC:H Dielectric Films. Francesca Iacopi[1], Carlo Waldfried[2], Thomas J. Abell[1,3], Eric P. Guyer[4], Brenda Eyckens[1], Youssef Travaly[1], Timo Sajavaara[1,5], David M. Gage[4], Gerald Beyer[1], Ivan Berry[2], Reinhold H. Dauskardt[4] and Karen Maex[1,6]; [1]IMEC, Leuven, Belgium; [2]Axcelis Technologies, Rockville, Maryland; [3]Intel Corp., Santa Clara, California; [4]Materials Science and Engineering, Stanford University, Stanford, California; [5]IKS, Katholieke Universiteit Leuven, Leuven, Belgium; [6]E.E.Dept, Katholieke Universiteit Leuven, Leuven, Belgium.

The introduction of considerable amounts of porous volume in dielectric films is the most effective route for achieving low-k materials for microelectronics, but it leads invariably to a substantial decrease of the mechanical strength of such films. This issue poses serious constrains onto the overall mechanical stability of low-k based interconnects. One ideal solution to enhance the stiffness of porous films and still preserve their low-k characteristics, would be to maximize the degree of cross-linking of the matrix material without affecting the porous volume. Exposure of dielectric films to UV radiation with appropriately chosen energy/wavelengths can be used to promote such cross-linking mechanisms in a controlled fashion, so to avoid significant film densification. This study looks into the effects of UV cure onto the properties of 300 to 700nm thick blanket microporous SiOC:H films with a pristine k value around 3.0. The most effective cure condition investigated leads to about 50% increase in elastic modulus and hardness. The same increase trends in elastic modulus are observed with both nanoindentation and Surface Acoustic Waves, although the SAWs values are typically 20-30% lower

than those from nanoindentation. Strain energy release rates upon fracture as measured with four-point bending show a clear increase for stacks containing UV-cured SiOC:H films. Only minor film shrinkage (~4%) and increase in film density (from 1.48 g/cm^3 to 1.52 g/cm^3) are associated with this cure condition, as well as a minor increase of the k value to about 3.15. Structural and compositional changes in the SiOC:H upon UV cure are studied by means of Heavy Ion Elastic Recoil Detection and solid state Nuclear Magnetic Resonance analysis.

11:30 AM B3.10
Effect of Plasma Treatment and TMCTS Vapor Annealing on the Reinforcement of Porous low-k Films. Kazuo Kohmura[1], Hirofumi Tanaka[1], Shunsuke Oike[1], Masami Murakami[1], Tetsuo Ono[1], Yutaka Seino[2] and Takamaro Kikkawa[2,3]; [1]MIRAI-ASET, Tsukuba, Japan; [2]MIRAI-ASRC-AIST, Tsukuba, Japan; [3]RCNS, Hiroshima, Japan.

The aim of the present study is to improve the elastic modulus of the porous silica films with keeping the k-value low. Introducing pores to silica films could reduce the k-value, while it is unstable in air because of water adsorption in mesoporous silica. We treated the porous silica film in 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS) vapor for improving the elastic modulus and the hydrophobicity. It is shown that the mechanical strength of the porous silica films was significantly enhanced by a novel process of TMCTS vapor annealing combined with a plasma treatment. The TMCTS treatment was performed at 400?C in nitrogen ambience followed by the argon plasma treatment under the pressure range of 0.3 to 2.0 Pa for 40 sec. The elastic modulus of the porous silica film with TMCTS treatment significantly increased after the plasma treatment. Furthermore, after the second TMCTS treatment was carried out; both the elastic modulus and the hardness of the film were enhanced by a factor of 4, as compared with those of the starting film. FT-IR analysis indicated that Si-CH3 and Si-H groups on the porous silica wall surfaces were converted to Si-OH groups after the argon plasma treatment, indicating that the pore wall surface became more reactive with TMCTS vapor after the argon plasma treatment. Thus the porous silica wall surface was covered by TMCTS polymer network and became more hydrophobic. Consequently the refractive index increased by about 5 % and the elastic modulus increased by a factor of 4, while k-value was kept almost constant.

11:45 AM B3.11
High Strength Low Dielectric Constant Aromatic Thermosets. Yongqing Huang and James Economy; Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois.

Continuing miniaturization of microelectronic devices requires development of low dielectric constant materials to lower the RC delay, power dissipation and crosstalk. Although spin-on polymer dielectrics have better potential for extendability to lower dielectric constant (k) values compared to chemical-vapor-deposited dielectrics, their low mechanical properties prevent them from being successfully integrated with copper metal lines. Recent evaluation of a new thermosetting oligomer shows high thermal stability, low moisture pick-up and low dielectric constant. Techniques to optimize the solubility and spin coating characteristics of the oligomer have been developed. The thermally cured polymer displayed a thermal stability up to 480°C in nitrogen and 400°C in air. The cured polymer displayed a dielectric constant of 2.7 at 1 MHz and a breakdown strength larger than 230 V/μm. Nanoindentation testing showed that it had an extraordinarily high Young's modulus of 16.8 GPa and a hardness of 3.5 GPa. By use of porogens, a dielectric constant as low as 1.85 was obtained while still maintaining an acceptable high Young's modulus of 7.7 GPa and hardness of 2.0 GPa. Nanoscratch testing indicated that this material had good adhesion to the Si substrate, and Ta which is a diffusion barrier for copper. These results appear unique compared to all commercially available low-k candidates.

SESSION B4: Reliability of Low-K Dielectrics
Chair: Tom Shaw
Wednesday Afternoon, March 30, 2005
Room 2004 (Moscone West)

1:30 PM *B4.1
Constraint Effects on Cohesive Failures in Low-k Dielectric Thin Films. Ting Y. Tsui and Andrew J. McKerrow; Silicon Technology Development, Texas Instruments Inc, Dallas, Texas.

With increasing demands on interconnect performance the semiconductor industry is replacing traditional BEOL dielectrics with materials characterized by a lower dielectric constant. At the 90 nm node organosilicate glasses (OSGs) are one class of materials that have been extensively evaluated as candidate intermetal dielectrics. A potential mechanical failure mode for these silicon-based, low-k dielectric thin films during interconnect fabrication is channel crack fracture, of which the major driving force is residual tensile stress in the film. Even if the film does not crack catastrophically immediately after deposition, time-dependent failures can occur via stress-corrosion cracking. This phenomenon is commonly referred to as environmentally-assisted crack growth. In this work, elastic constraint effects of underlying films or film stacks on crack growth rates of OSG thin films were characterized. It is demonstrated that the strain-energy-release-rate and crack growth velocity of low-k dielectric depended strongly on the elastic properties and thickness of the under-layer materials. Furthermore, it was found that the crack growth rate increased by a power law function with under-layer thickness, if the material is more compliant than OSG. This poses challenges to future BEOL mechanical reliability, since next generation ultra low k dielectrics are expected to be more compliant and fragile than the materials used for the 90 nm technology node. To demonstrate this, a five-metal-layered dielectric stack was built using an ultra low-k dielectric, and crack velocity measurements made for an OSG film deposited on top of this stack. Results show that crack growth rate was 10,000 times faster than the equivalent experiment performed on a film stack prepared using low-k dielectrics. The implication of this significant increase in crack opening force will be discussed.

2:00 PM B4.2
Integration and Reliability Issues Using Novel ULK Spin-on Dielectric Schemes. Neil Henis[3,4], Klaus Pfeifer[3], Gregory Smith[3], Ward Engbrecht[3,1], Sanjit Das[3,2], Kyle Neuman[3] and Mike Gallagher[5]; [1]Texas Instruments, Dallas, Texas; [2]IBM, Hopewell Junction, New York; [3]SEMATECH, Austin, Texas; [4]Freescale Semiconductor, Austin, Texas; [5]Rohm and Haas, Marlbourough, Massachusetts.

Reliability (BTS/EM/SM) of various integrations of porogen activated mesoporous ULK spin-on ILD/hard mask (kint=2.5) are examined. Correlations are drawn between ramped breakdown voltage, packaged and wafer level reliability testing methods. A promising ULK scheme is shown and discussed. Wafer level BTS measurements are made in a tester with a 300mm thermally controlled chuck, at temperatures ranging from 25-300C, and voltages ranging from 12-23V. Packaged BTS data was run in either hermetically sealed packages, or in an N2 ambient at 250C/15V. Integration schemes tested included ILD/low k organic etch stop layer, and ILD/spin on silsesquioxane hard mask. Various barrier thicknesses were also tested in the integrations. A good correlation between leakage at low voltages in the ramped breakdown voltage tests on syst structures, and lifetimes at temperature in BTS is found. With the proper integration scheme, high reliability can be achieved with an ultra low-k process flow.

2:15 PM B4.3
Study of the Kinetics of Cu Oxidation in SiO2 using Solid-State Impedance Spectroscopy. Oscar Rodriguez, Woojin Cho, Ravi Saxena, William N. Gill and Joel L. Plawsky; Department of Chemical and Biological Engineering, Rensselaer Polytechnic Institute, Troy, New York.

This work is aimed at understanding the nature of the interactions between metal interconnects and SiO2 in integrated circuits. Cu diffuses readily in SiO2 and Si creating a reliability concern. The mechanism of Cu diffusion in SiO2 and low-k dielectrics is still a matter of controversy. We have shown that the diffusion of Cu in inorganic dielectrics depends strongly on the moisture content and defect concentration of the dielectric. In this paper we study the time dependence of Cu oxidation in SiO2 using solid-state impedance spectroscopy. In an experiment, bias-thermal-stressing is applied to Metal-Insulator-Capacitors to induce oxidation and diffusion of Cu mobile charges into the dielectric. The frequency response of the dielectric layer is studied before and after stressing. An equivalent circuit model to describe the system is developed and constants for the dynamics of Cu diffusion at the interface and bulk of the dielectric are derived.

2:30 PM B4.4
Barrier Integrity Effect on Leakage Mechanism and Reliability of Copper/OSG Interconnects. Yunlong Li[1,2], Zsolt Tokei[1] and Karen Maex[1,2]; [1]IMEC, Leuven, Belgium; [2]Department of Electrical Engineering, Katholieke Universiteit, Leuven, Leuven, Belgium.

With the introduction of low-k dielectric into on-chip interconnects, leakage under use condition is becoming a significant reliability concern. Possible leakage paths in copper damascene structure include the one through bulk dielectric plus copper diffusion barriers and other integration interfaces. In this paper, the dominant leakage path is restricted to the former one by modulating the barrier integrity: sealing and sub-critical barriers are compared. The low-k is a micro porous organo silicate glass (OSG, k=3). In TDDB measurements,

significant difference in both extrapolated lifetimes and temperature acceleration were found for different barrier treatments. Close to zero thermal activation energy is expected for ideal non-contaminated OSG. Voltage ramp measurements were used to investigate the conduction in detail. Regardless of barrier treatment, the I-V curves on 'fresh' devices fit well with a Frenkel-Poole emission mechanism above 1.4MV/cm between 20C and 200C. The extracted Coulombic potential trap height is 1eV. Constant current stress (CCS, 200pA) with different stress times is applied at 100C, during which higher voltage is required to induce the same current for structures with a sub-critical barrier. This shows the internal potential reduction caused by copper ions in OSG. After 50s CCS the structure with a sub-critical barrier has more than 1 order of magnitude higher leakage at 0.07 MV/cm than the one with a sealing barrier pointing to ionic contribution of copper. Above 1.4 MV/cm the detected leakage current for a porous barrier is significantly lower due to a higher trap density induced by the presence of copper. The slope of I-V curves at high field keeps constant independent of stress time. For voltage ramp following different CSS times on sealing barriers, strictly no difference is detected below 3.0MV/cm. In summary, sub-critical barrier can change the low-field leakage to ionic conduction and the drifted copper ions will significantly degrade the dielectric. But the leakage mechanism at high field is the same regardless of the amount of captured copper ions. Copper ions, however, accelerate the formation of defective sites in OSG. Thus for sub-critical barriers, a percolation path of defective sites can be formed in a shorter time and leads to faster dielectric degradation.

2:45 PM B4.5
Kinetics of Moisture-Induced Electrical Property Changes in Ordered Nanoporous Silica Low-k Dielectric Thin Films.
A. P. Singh, P. Victor, P. G. Ganesan and G. Ramanath; Materials Science & Engineering, Rensselaer Polytechnic Institute, Troy, New York.

Introducing porosity into insulating materials is a promising strategy to decrease the dielectric constant to minimize RC delays in microdevice wiring. However, the lack of adequate control on porosity size, shape, and surface passivation can lead to inferior mechanical integrity and chemical instabilities due to processes such as moisture uptake. Here we report the synthesis, electrical properties, and moisture-induced chemical instabilities of a nanoporous low-k silica xerogel with an ordered array of nanoscale pores. Based upon our results, we propose a kinetic model describing the chemical instabilities and suggest a strategy to obviate the instabilities. Silica xerogels with ordered pores were synthesized by a sol-gel technique using tetraethylorthosilicate (TEOS) and micellar templates comprised of Brij56-a non-ionic surfactant Transmission electron microscopy (TEM), ellipsometry and capacitance voltage measurements of spin-coated xerogels on silicon substrates reveal uniform films of controllable thickness between 100 to 250 nm, a dielectric constant of 2.4 and $>$ 4 MV/cm breakdown field. These properties make this material a promising candidate for interlayer dielectrics in metallization structures. Annealing the Al/xerogel/Si/Al metal-oxide-semiconductor (MOS) capacitors from 80 to 140 ^{o}C for time intervals between 2 to 120 min decreases accumulation capacitance and alters the flat band voltage hysteresis along with a gradual disappearance of an initially observed deep-depletion region. The flat band hysteresis width initially increases, and decreases upon further annealing after going through a maximum. Kinetics analyses of the loop hysteresis electrical signatures yield activation energy of 0.39 $\pm$ 0.05 eV, consistent with surface diffusion of water in silica and activation energy 0.54$\pm$0.05 eV, which is attributed to H^{+} migration in silica. The physical phenomena attributed to these activation energy values are confirmed by infrared spectroscopy measurements of annealed samples showing absence of Si-OH and -OH stretching. Based upon our results, we present an atomic-level phenomenological kinetic description of the instabilities, and suggest a strategy to immunize the porous structure against moisture-attack.

SESSION B5: Copper Interconnects
Chair: Christine Hau-Riege
Wednesday Afternoon, March 30, 2005
Room 2004 (Moscone West)

3:30 PM *B5.1
Continued Scalability of Copper low-k Interconnects.
Sywert Hidde Brongersma[1], Laureen Carbonell[1], Kris Vanstreels[2], Francesca Iacopi[1], Jan D'Haen[3], Wenqi Zhang[1], Youssef Travaly[1], Steven Demuynck[1], Zsolt Tokei[1], Ward DeCeuninck[2,3] and Karen Maex[1,4]; [1]SPDT/ITTO, IMEC, Leuven, VB, Belgium; [2]Institute for Materials Research, Limburgs Universitair Centrum, Diepenbeek, Limburg, Belgium; [3]IMOMEC, IMEC, Diepenbeek, Limburg, Belgium; [4]E.E.Dept, Katholieke Universiteit Leuven, Leuven, VB, Belgium.

As modern copper/low-k interconnects continue to scale, both the dielectrics and metallization face increasing challenges beyond the 90 nm node. For dielectrics, a further reduction of the k-value nescessitates the introduction of porosity. This puts stringent requirements on both sealing techniques and mechanical integrity. In order to minimize compromizing effects on the effective k-value, processing damage and sidewall sealing need to be sufficiently (and increasingly) shallow. As the effective resistivity of interconnect lines continues to increase with decreasing dimensions, optimization and novel solutions are needed for both barrier and copper microstructure. These include ALD, overburden ingrowth, plating chemistry and processing parameter changes, novel filling mechanisms, and a new growth mode known as super-secondary-grain-growth. The most promising integratable and scalable solutions will be highlighted.

4:00 PM B5.2
Structure Evolution in Plated Cu Films.
David P. Field[1], No-Jin Park[1,4], Paul R. Besser[2] and John E. Sanchez[3]; [1]Washington State Univ, Pullman, Washington; [2]Advanced Micro Devices, Sunnyvale, California; [3]Unity Semiconductor, Sunnyvale, California; [4]Kumoh National Institute of Technology, Kumi, South Korea.

Optimization of interconnect microstructure for improved manufacturability and reliability has long been a subject of ongoing research, initially for Al structures and now for Cu metallization. This research remains critical as minimum feature sizes continue to shrink in increasingly complex integrated circuits. Failures in Cu interconnects, either stress induced or from electromigration processes, are likely a function of the Cu microstructure that evolves during processing. Optimization of this structure requires an understanding of both structure/property relationships as well as microstructural evolution during processing. As typical interconnects go through many processing steps that involve temperatures up to 400 deg C or more, it is important to understand the effects of elevated temperature on the evolution of Cu microstructures. This structural evolution is a function of sublayer materials and thicknesses, bath chemistry for electroplated films, and initial deposition conditions. Electron backscatter diffraction analysis of Cu films processed by various methods reveals differences in microstructural evolution during in-situ annealing.

4:15 PM B5.3
Accelerated ECP Process Development with Automated Cu Grain Boundary Analysis Using SEMVision G2 FIB.
Vicky Svidenko[1], Roman M. Mostovoy[2], Aron Rosenfeld[2], Laurent Karsenti[1] and Lior Levin[1]; [1]PDC, Applied Materials, Inc., Santa Clara, California; [2]TFG, Applied Materials, Inc., Santa Clara, California.

The Cu grain size distribution and morphological analysis has increasingly become one of important parameters impacting interconnect resistivity, electromigration and stress migration (EM/SM) device reliability in the Cu interconnect era. There is a need for a robust and automated grain boundary (GB) characterization mechanism in the earliest stages of process development. SEMVision G2 FIB is an automated dual beam SEM and FIB tool which enables enhanced visibility of grain boundaries by focused ion beam (FIB) sputtering right after copper plating. The sputtered area is imaged with a high resolution scanning electron microscope (SEM). QPM (Quantified Process Monitoring), a novel automated application on the SEMVision G2 FIB, is used to analyze the SEM images and yields a grain boundary (GB) density result. The GB density under a wide variety of process conditions such as anneal temperatures and different plating recipes along with wafer level (center to edge) uniformity can be easily characterized and monitored with this simple and robust technique. Another major advantage of the GB analysis is its capability to perform Cu grain boundary metrology on dense pattern, where it matters most for parametric and reliability performance. This capability opens new directions to accelerate process development and improve EM/SM device reliability. The experiments described in this paper explored the impact of a wide range of pulse ECP frequencies and amplitudes, as well as a wide range of post-ECP in-situ anneal temperatures and durations on copper film grain boundary density and sheet resistance. For the pulse plating experiment, the baseline process, together with a 10Hz pulse plating process yielded the lowest GB density. Higher frequency pulse plating caused a rapid increase of GB density as well as significantly higher variance in GB density on wafers plated with 50Hz ? ? ? 200Hz. No sensitivity of GB density to the pulse amplitude was observed. In the anneal experiments, for a one-step (30 sec) anneal, the GB density decreased with increasing anneal temperature. Two-step anneal processing decreased the GB density significantly. The lowest GB density was achieved with 1 hour anneal at 250C.Copper GB density had a very high correlation to electrical sheet resistance, as measured by the four-point-probe method. In addition, we characterized the dependence of grain boundary on Cu

feature size and showed a systematic increase in GB density with decreasing feature size. Automated copper GB analysis on the SEMVision G2 FIB is an example of a process metrology application jointly developed by process diagnostics and copper plating R&D teams, tailored for the unique advanced process control needs of the ECP process. This automated metrology has the potential to shorten the learning cycle in ECP process development. This analysis offers in-line ECP process monitoring capability, and should significantly enhance device EM/SM testing outcomes.

4:30 PM B5.4
The Effect of Temperature on Spontaneous Morphology Change in Electrodeposited Copper Metallization.
Shafaat Ahmed[1], D. N. Buckley[1], S. Nakahara[1] and Y. Kuo[2]; [1]Department of Physics, Materials and Surface Science Institute,University of Limerick, Limerick, Ireland; [2]Department of Chemical Engineering, Texas A&M University, College Station, Texas.

The results of a detailed investigation by atomic force microscopy (AFM) of the nanostructure and morphology of electrodeposited copper metallization and its evolution with time is presented. Copper films were galvanostatically electrodeposited on various substrates from acidic CuSO4 baths. A spontaneous morphology change (SMC) was observed in real time by in situ AFM during room temperature aging of these films. The phenomenon involves the formation, usually quite suddenly, of new features, smaller than the existing features on the surface. It has been shown that this occurs in copper films electrodeposited under many different conditions and is quite reproducible. The actual morphological change event was captured in real time when it occurred during the scan of an AFM image and the density of smaller surface features was observed to increase rapidly with time as indicated by the variation from top to bottom in the micrographs. Measurements of surface roughness obtained from AFM images showed a similar increase during SMC. An incubation period was observed between the end of electrodeposition and the onset of SMC. The length of the incubation time was found to depend on the temperature. It is assumed that a process, which we call recovery, occurs in the film during the incubation period at a temperature-dependent rate. A systematic investigation of annealing time and temperature was carried out. A series of films were deposited and, beginning a short time (~20-35 s) after electrodeposition, each sample was annealed by immersion in a thermostatted bath for a predetermined period of time. The sample was then removed from the bath and, after rinsing and drying, AFM images of the surface were scanned repeatedly until SMC was observed. Samples were annealed for various times at each of a series of temperatures and the total time after electrodeposition at which SMC occurred was noted for each sample. In experiments at a given value of annealing temperature, values of the remaining incubation time at room temperature were observed to decrease linearly as the annealing time was increased. The measured rates of decrease gave a linear Arhennius plot. After appropriate iteration to correct for variations in room temperature, the Arhennius analysis gave a value of 0.48 eV for the activation energy of the recovery process. It is proposed that the phenomenon of SMC arises from a volume contraction in the copper film due to the out-diffusion of excess vacancies. This leads to a tensile stress in the near-surface region. At some critical thickness, the near-surface region can no longer retain the elastic stress, it loses its elastic coherency and surface undulation occurs to relieve the stored elastic energy. The observed activation energy is consistent with this mechanism.

4:45 PM B5.5
Cu Resistivity in Narrow Lines: Effect of Metallization Scheme.
Sylvain Maitrejean[1], Anne Roule[1], Jean-Frederic Guillaumond[1,2], Murielle Fayolle[1], Anthony Roman[2], Thierry Morel[1], David Bouchu[1], Paul-Henry Haumesser[1], Lucile Arnaud[1] and Gerad Passemard[2]; [1]CEA-LETI, Grenoble, France; [2]STMicroelectronics, Crolles, France.

In order to reduce RC delay and to enhance electromigration resistance of device interconnects, Cu has been introduced in the late nineties, replacing Al alloy lines. Nowadays, as interconnects critical dimensions reach values under 100nm, an increase of Cu resistivity has been observed in narrow lines. This can be attributed either to higher electron scattering along grain boundary and Cu/barrier interfaces in small dimension and to an increase of impurity content in narrow lines. This works is conducted to understand metallization scheme impact on resistivity. Narrow trenchs are performed by deposition of a conformal PECVD dielectric liner on standard patterned structures (back fill techniques). Trench widths down to 50nm are thus obtained. Several metallization schemes have been optimized to properly fill these small features: Cu Barrier / Cu seed layer stacks can be either PVD TaNTa/PVD Cu, MOCVD TiN/MOCVD Cu or PVD TaNTa/Electrochemical Cu Seed. Cu fill is performed by electrochemical deposition (ECD). Chemistries with high or medium acid level are used. Finally, various Cu anneals are achieved.. Cu grain size is characterized with respect to line width and metallization scheme. Cu crystallographic orientation is evaluated. Electrical measurements are conducted to determine Cu resistivity versus line width. For each metallization, good Cu filling is obtained. Moreover, electrical data show good within wafer uniformity. As expected, Cu resistivity dramatically increases for line dimensions below 150nm. Concerning the impact of metallization scheme on resistivity, minor effect of ECD Cu fill chemistry and Cu anneal is observed whereas high Cu resistivity variations are obtained with respect to barrier/Cu Seed stacks. Lowest resistivity is measured for structures using MOCVD TiN/MOCVD Cu barrier/seed. It is worth to notice that this behavior is line width independent. These results are correlated with grain size measurements and textural characterization of the patterned structures.

SESSION B6: Barrier Metal Films
Chairs: Sywert Brongersma and David Field
Thursday Morning, March 31, 2005
Room 2004 (Moscone West)

8:30 AM B6.1
Atomic Layer Deposition (ALD) of Barrier/Adhesion/Seed Layers for Interconnects.
Zhengwen Li[1], Huazhi Li[1], Youbo Lin[2], Roy G. Gordon[1] and Joost J. Vlassak[2]; [1]Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts; [2]Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts.

ALD was used to deposit highly uniform and conformal diffusion barriers of tungsten nitride (WN), adhesion layers of ruthenium or cobalt, and copper seed layers. All ALD steps were done under reducing conditions in the absence of oxygen. The reactions are thermally activated without any plasma. Composition and thickness of the layers were determined by RBS, XPS and TEM. Conductivity measurements were made during growth, as well as after post-growth anneals. Adhesion was evaluated by four-point bend tests. Comparisons will be made between the thermal stability, conductivity and adhesion of multi-layers made with Ru or with Co.

8:45 AM B6.2
MOCVD of Highly Conformal Cobalt Metal Films.
Jeonggil Lee, Heejung Yang and Jaegab Lee; School of Advanced Materials Engineering, Kookmin University, Seoul, South Korea.

Co2(CO)8 produced the pure Co films with negligible contamination, showing low resistivity of about 6 $\mu\Omega$-cm after annealing at 400°C. However, the degraded conformal deposition of Co films has been obtained at the temperature between 200 and 400°C, possibly due to the gas-phase reaction between the molecules. Lowering the temperature significantly improved the conformality, and thus developing a very low temperature CVD processing for highly conformal deposition of pure Co films over high aspect ratio (30:1) trenches using cobalt carbonyls (Co2(CO)8) as the precursor. In addition, the temperature regime reveals the activation energy of about 0.8 eV. Further, the as-deposited Co films exhibited the low resistivity of 12 $\mu\Omega$-cm, which dropped to 8 $\mu\Omega$-cm after annealing at 400°C. Oxygen and carbon contamination were within AES detection limits. These films appear to be suitable as adhesion/seed layers in copper interconnects and for a low temperature processing of a variety applications with complex structures.

9:00 AM B6.3
Atomic Layer Deposition of Ruthenium Thin Films for the 45-nm Era.
Jin Yong Kim[1], Sang Yeol Kang[1], Beom Seok Seo[2], Jung Hyun Lee[2], Kwanghee Lee[1], Han Jin Lim[1], Cha-Young Yoo[1], Sung-Tae Kim[1], U-In Chung[1] and Joo-Tae Moon[1]; [1]Process Development Team, Samsung Electronics Co., Ltd., Yongin-Si, Gyeonggi-Do, South Korea; [2]Nano Fabrication Center, Samsung Advanced Institute of Technology, Yongin-Si, Gyeonggi-Do, South Korea.

As the semiconductor industry heads toward the 45 nm technology node, the need for conformal and conductive barrier layer for copper has led the atomic layer deposition (ALD) technique to be a promising alternative to conventional physical vapor deposition (PVD) techniques. ALD-ruthenium has shown great promise to plate copper directly onto a diffusion barrier. Not only could ruthenium potentially replace a two-step Ta/TaN process commonly used for diffusion barriers, but it could replace the seed layer as well. One of the most widely researched applications of ruthenium thin film is a capacitor electrode in memory devices such as gigabit DRAMs and FRAMs. Another potential application of ruthenium is a PMOS metal gate electrode in conjunction with high-k gate dielectric films. However, it was shown that very thin ruthenium layer may not be adequate as a copper diffusion barrier. Hence, ruthenium film composition, morphology, adhesion characteristics, and step coverage should be optimized to meet the requirements. In this study,

ruthenium thin films were deposited using a remote-plasma-assisted ALD (RPALD). Various organometallic precursors of ruthenium such as $Ru(EtCp)_2$, Ru(DER), Ru(BuCp)Cp, $Ru(nbd)(iHD)_2$ were used as precursors, which were diluted with solvents and delivered into the reactor. Both oxygen and hydrogen were alternatively fed into the reactor as reactant gas through the remote plasma unit. Compared to conventional ruthenium CVD, the RPALD successfully overcame ruthenium nucleation issues on dielectrics without a PVD-Ru seed layer. A conformal step-coverage at the aspect ratio higher than 10:1 was obtained below the deposition temperature of 350 °C. The impact of deposition conditions such as temperature, plasma power, gas flows and reactant gas on film properties was studied.

9:15 AM B6.4
Plasma-Assisted Atomic Layer Deposition of TiN Films at Low Process Temperature in High-Aspect Ratio Structures.
S. B. S. Heil[1], E. Langereis[1], F. Roozeboom[2], A. Kemmeren[2], N. P. Pham[3], P. M. Sarro[3], M. C. M. van de Sanden[1] and W. M. M. Kessels[1]; [1]Applied Physics, Eindhoven University of Technology, Eindhoven, Netherlands; [2]Philips Research, Eindhoven, Netherlands; [3]Delft University of Technology, Delft, Netherlands.

Titanium nitride (TiN) has an important application as diffusion barrier and metallization layer in via interconnects. TiN films can be deposited in high-aspect ratio structures by atomic layer deposition (ALD) in which the best material properties (low resistivity, low contamination level, etc.) are obtained by using metal halide precursors. Due to copper pitting, these precursors can only be used at low processing temperatures (<200 °C) that can be achieved when using a plasma step for ligand abstraction. This so-called plasma-assisted atomic layer deposition (PA-ALD) might also enable higher deposition rates. The work presented here focuses on PA-ALD of TiN in high-aspect ratio features using $TiCl_4$ precursor dosing and hydrogen/nitrogen plasma exposure. In situ spectroscopic ellipsometry has been used to map out the ALD parameter space in terms of precursor dosing, plasma exposure, and substrate temperature dependence. Besides thickness information, these in situ measurements have also revealed insight into the film properties such as electrical resistivity and mass density. Furthermore, the conditions yielding optimum film properties have been identified by nuclear profiling measurements and X-ray diffraction yielding the composition of the films and their microstructure. The conformality of the films has been studied in macropore (aspect ratio of 20:1) and open via structures (aspect ratio up to 50:1) using a combination of SEM and cross-sectional TEM imaging. At low process temperatures the TiN tends to be less polycrystalline which makes it better suited for diffusion barrier applications. Furthermore, the Cl-impurity level remains low (<1 at.%) at a process temperature of 200 °C while the resistivity of ~200 $\mu\Omega$·cm is sufficient for the film to act as seed layer during copper electroplating of the open via interconnects.

9:30 AM B6.5
Integration of ALD-TaN Liners on Nanoporous Dielectrics.
Bum Ki Moon[1], Tadashi Iijima[2], Sandra Malhotra[3], Andrew Simon[3], Thomas Shaw[3], E. Todd Ryan[4], Cathy Labelle[4], Nick Fuller[3], Tibor Bolom[4], Keishi Inoue[5] and Vincent McGahay[3]; [1]Infineon Technologies, NA, Corp., Hopewell Junction, New York; [2]Toshiba America Electronic Components, Inc., Hopewell Junction, New York; [3]IBM Microelectronics, Hopewell Junction, New York; [4]AMD Corp., Hopewell Junction, New York; [5]Sony Electronics Inc., Hopewell Junction, New York.

Ultra-thin TaN liners have been developed to prevent Cu diffusion into porous interlayer dielectric (ILD) materials envisioned for future copper interconnections. In order to get an ultra-thin and conformal layer, TaN films are prepared using atomic layer deposition (ALD). The porous ultra-low k (p-ULK) film is prepared using the spin-on method, and then ALD-TaN is deposited on both patterned and blanket p-ULK films. The typical k-value and the average pore size of p-ULK used in this paper are 2.3 and 2-3 nm, respectively. The pores are completely interconnected. Interaction and phenomena at the ILD/ALD-TaN interface have been investigated and the electrical measurements were performed after completing the metallization and CMP process. For the case of as-deposited p-ULK films, a deep penetration of ALD-TaN was observed. This is because the pores are interconnected, and the ALD precursor vapor can diffuse through them into the bulk of the film easily. In order to avoid the direct diffusion, an additional layer is needed to the seal pores in the p-ULK film prior to atomic layer deposition of liners. However, TEM shows that the surface of the p-ULK is drastically changed after the etch process, where changes are attributed to plasma damage and re-deposition of etched species onto the sidewall. Most of the pores along the trench sidewall can therefore be sealed during the etch process. Furthermore, the plasma damage makes the sidewall more hydrophilic, and this hydrophilicity may reduce the incubation time of the ALD TaN layer on the etched surface. Based on electron energy loss spectroscopy (EELS) and EDS profiles across the liner/ILD interface, there is no signature of TaN penetration into the etched p-ULK at M1 level. From the EDS line profiles, a sharp Ta peak was observed at the interfaces with p-ULK and Cu, which indicates excellent stability of ultra-thin ALD-TaN liner. An oxidation test in air ambient and at elevated temperature confirmed the barrier properties of the stacked ALD-TaN/Ta layers. Oxygen diffuses through the pores of p-ULK to the interface of TaN. Any weak point in the TaN/Ta barrier allows the Cu to oxidize, which is easily detected by a color change under an optical microscope. All of our samples showed no color change due to Cu oxidation, which implies that the barrier is very uniform and stable on the sidewall. Electrical properties measured at M1 using a comb structure showed an excellent results. Typical short and open current values were 10^{-9} A and 10^{-7} A, respectively. Also, the Rs yield was 100%, even for a sample with a 1.5nm thick TaN layer. Our results demonstrate the ability to successfully integrate ALD-TaN barriers with a nanoporous ULK film. – This work is supported by the independent alliance programs for SOI technology development and Bulk CMOS technology development.

10:15 AM B6.6
Effect of Dielectric Pore Size Distribution on Interfacial Adhesion of the Ta-Porous Dielectric Interface.
Ravi Saxena[1], Woojin Cho[1], Oscar Rodriguez[1], Ting Tsui[2], Stephan Grunow[2], William N. Gill[1] and Joel Plawsky[1]; [1]Chemical Engineering, Rensselaer Polytechnic Institute, Troy, New York; [2]Texas Instruments, Dallas, Texas.

An important reliability issue facing the integration of porous low-k dielectric substrates in microelectronics is the effect of dielectric porosity and pore size distribution on the adhesion properties of contiguous barrier (tantalum) layers. As these layers get thinner and dielectric get more porous, they lose adhesion upon processing leading to disastrous consequences for circuit performance. This work examines the underlying mechanisms that result in compressed barrier-film delamination and their dependence on porous dielectric internal properties, namely the pore size distribution and chemistry. The high compressive stresses in the barrier layers (Ta) lead to delamination from the underlying substrate if the stress energy exceeds the interfacial adhesion energy. If the delamination is spontaneous, it results in the formation of telephone-cord like morphologies, which allow the measurement of critical adhesion (fracture) energy. In cases where spontaneous delamination does not occur, the interfacial fracture energy is determined by industry standard methods like 4 point-bending. The interfacial adhesion of Ta to a variety of porous dielectrics with varying pore size distribution is determined using the two tests. The chemistry of the delamination interface is characterized using depth XPS. It was found that interfacial adhesion depends inversely to the square of underlying dielectric pore size. Strong correlation was found in the dielectric chemistry, porosity, pore size distribution and the fracture energy. The mechanisms of such a correlation will be discussed.

10:30 AM B6.7
Picosecond Ultrasonic Characterization of Ultrathin Bilayer Films with Graded Interfaces.
Michael Kotelyanskii, Eugene Terentiev, Guray Tas, Christopher Morath and Jana Clerico; Rudolph Technologies, Flanders, New Jersey.

The use of thin bilayer films with a graded interface is common in semiconductor manufacturing. For example, Ti and its nitride are well known barriers for Al-SiO2 process and Ta, W, and their nitrides are heavily used as barriers for the Cu-Low K dielectric processes. Generally, the deposition of these films starts with the metal film and then nitrogen is introduced into the chamber to create a smooth and continuous transition to nitride. Picosecond ultrasonics (MetaPULSE) was used to characterize these types of sequentially deposited bilayer films. The measurements were compared with the calculations from a physical model that accurately describes sound generation and both light and sound propagation in thin films with gradually varying properties. Thickness and composition profiles were determined by optimizing model parameters to find the best fit to the measured data.

10:45 AM B6.8
Managing Composition and Properties of CVD Boron Carbo-Nitride Films.
P. Ryan Fitzpatrick[1], Edward R. Engbrecht[1,2] and John G. Ekerdt[1]; [1]Chemical Engineering, Univ of Texas at Austin, Austin, Texas; [2]Silicon Technology, Texas Instruments, Dallas, Texas.

Thin (10-100 nm) films of boron carbo-nitride (BC_xN_y) were grown by chemical vapor deposition (CVD) for potential use as copper diffusion barriers between copper interconnect lines and the interlayer dielectric. Films were grown using dimethylamine borane as the CVD precursor with no coreactant, ethylene, or ammonia. Adjusting the coreactant gas choice and flowrate allowed for a tunable film composition and dielectric constant, k. When ethylene was used as a

coreactant at 360°C and 1 Torr, films of $BCN_{0.1}$ stoichiometry were grown with k values less than 4. Four-point bend test results indicated that BC_xN_y films strongly adhere to dielectric films (composite beams snapped during testing). The critical debond energy changed with BC_xN_y composition; films grown with dimethylamine borane and ethylene did not delaminate when deposited on the oxidized Cu surface. The copper diffusion barrier properties were studied using bias-temperature stress testing at 150°C and 2 to 5 MV/cm of metal-insulator-semiconductor (MIS) test structures. The samples were analyzed for the time-to-failure (TTF) under a given electric field. A $SiC_{0.76}N_{0.44}$ film was used to benchmark the study. $BC_{0.90}N_{0.08}$ deposited using ethylene was the most promising boron-based film, having a k less than 4, leakage current of 1.12×10^{-8} A/cm^2 at 0.5 MV/cm (compared to 5.50×10^{-9} A/cm^2 for $SiC_{0.76}N_{0.44}$), and time-to-failure performance comparable to $SiC_{0.76}N_{0.44}$. BC_xN_y films were also investigated for their potential use as a capping layer for porous ultra low-k interlayer dielectrics to prevent infiltration of organometallic precursors. Preliminary results indicate that approximately 2 nm $BC_{0.1}N_{0.5}$ blocks tetrakis(dimethylamino)titanium precursor penetration during a 15 min exposure to the titanium precursor at 200°C, as revealed by XPS depth profiling.

11:00 AM B6.9
Molecular Layers for Inhibiting In-Plane Surface/Interfacial Cu Diffusion in Damascene Interconnects.
Chandrasekar Venkataramani[1], P. G. Ganesan[2], Anand V. Vairagar[1,3], G. Ramanath[2], Subodh G. Mhaisalkar[1] and Ahila Krishnamoorthy[3]; [1]School of Materials Engineering, Nanyang Technological University, Singapore, Singapore, Singapore; [2]Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York; [3]Semiconductor Process Technologies, Institute of Microelectronics, Singapore, Singapore.

The use of Cu wiring with interlayer isolation provided by low-k materials is the state-of-the-art technology for interconnect devices in integrated circuits. However, problems such as Cu transport across Cu-dielectric interfaces, which also show poor adhesion persist, and must be addressed. Self assembled molecular layers have been shown to be attractive for addressing both these problems. Here, we show that molecular layers can be used to inhibit leakage currents driven by in-plane diffusion of Cu along Cu-dielectric interfaces. Leakage current measurement was carried out on molecularly passivated single-damascene interdigitated comb structures comprised of 400 Cu lines each of which had a 1000 m length. The trenches were filled with 25 nm Ta by sputter deposition followed by electroplating of Cu, and excess metal in the field areas was removed by Chemical mechanical planarization. Organosilane molecular layers of three different termini, namely, thiol, amino-phenyl and amino propyl were formed to cap the surfaces from millimolar solutions in toluene. X-ray photoelectron spectroscopy analyses reveal that the silane termini attached to the exposed silica regions while the amine and thiol functionalities are anchored onto the Cu layer, forming an upside down layer on the types of surfaces. Leakage current characteristics measured as a function of electric field varied between 0 to 1.4 MVcm-1 reveal that the aminophenyltrimethoxy silane is the most efficient inhibitor of in-plane leakage. Thiol-terminated organosilanes showed worse characteristics compared to even samples without any molecular passivation. These results are exactly contrary to the efficacy of these molecules in inhibiting Cu transport across Cu-SiO2 interface.

11:15 AM B6.10
Diffusion Barrier Properties of Carboxyl- and Amine-Terminated Molecular Nanolayers. P.G. Ganesan[1,2], A.P. Singh[1] and G. Ramanath[1]; [1]Department of Materials Science and Engineering, Renesselaer Polytechnic Institute, Troy, New York; [2]Center for Integrated Electronics, Renesselaer Polytechnic Institute, Troy, New York.

Devising sub-5-nm-thick barriers to inhibit Cu diffusion into dielectrics is a major challenge for sub-50 nm devices due to difficulties in realizing conformal films of conventional barriers, particularly in high aspect ratio non-planar geometries. Although advanced techniques such as atomic layer deposition show promise to overcome these difficulties, presence of crystalline defects and interface mixing are major concerns with conventional solutions. We have recently demonstrated that molecular nanolayers have attractive attributes for inhibiting Cu diffusion and enhancing interfacial adhesion. Here, we demonstrate carboxyl moieties grafted on amine-terminated self-assembled molecular layers (SAMs) to immobilize Cu at the Cu/SiO_2 interface. We also show that the molecular layer barrier properties are superior to that of sputter-deposited Ta layers of similar thickness. Amino-propyl-trimethoxy-silane (APTMS) nanolayers were formed on thermally oxidized silicon substrate by wet-chemical self-assembly from millimolar solutions of the molecules in toluene. We used bias annealing test at 200 °C, 2 MV/cm, to characterize barrier properties of the molecular layers. APTMS SAMs at the Cu/SiO_2 interface increase the Cu diffusion-induced device failure time by a factor-of-3 compared to interfaces without a barrier. Carboxyl-terminated SAMs obtained by grafting succinyl chloride onto the APTMS SAM show more than an additional factor-of-4 increase in failure time. X-ray photoelectron spectroscopy analyses reveal that the effective immobilization is mainly due to interface specific interaction between carboxyl moieties and copper. Coordination complex formation through strong interactions between COOH and Cu^+ at the Cu/SAM interface is the likely reason for the effective immobilization of Cu. We finally benchmark the barrier properties of the molecular nanolayers with that of conventional sputter-deposited Ta and TaN barriers. Our results show that molecular layers barriers are superior by a factor-of-2 compared with sputter-deposited Ta layers of similar thickness. The reasons for this behavior are discussed in terms of interface chemistry and structure obtained by XPS and cross-sectional TEM measurements.

11:30 AM B6.11
Thermal Oxidation of Cu Interconnects Capped with CoWP.
Jeff Gambino[1], Sean Smith[3], Steve Mongeon[1], Dave Meatyard[1], Fen Chen[1] and Pat DeHaven[2]; [1]IBM Microelectronics, Essex Junction, Vermont; [2]IBM Microelectronics, Hopewell Junction, New York; [3]IBM Thomas J. Watson Research Center, Yorktown Heights, New York.

The thermal oxidation of Cu interconnects has been studied as a function of thickness of the CoWP capping layer. For thin CoWP layers (25 nm), a thick (200 nm) oxide layer grows on the surface of the Cu line after a 350C, 5 m oxidation in air. The oxide is mainly composed of Cu2O, with a thinner CoO layer underneath. Some CoWP (about 5 nm) remains after oxidation and there is no significant oxygen in the underlying Cu. For thick CoWP layers (50 nm), the oxide layer is much thinner (36 nm) and is mainly composed of CoO. The remaining CoWP is about 27 nm thick and there is no significant oxygen in the CoWP or the underlying Cu. For both CoWP thicknesses, depletion of the underlying Cu is often observed after oxidation and whisker growth is often observed on the surface. The results are consistent with an oxidation mechanism where metal is the dominant diffusing species. For thin CoWP layers, Cu diffuses more quickly to the surface than Co, and therefore mainly Cu oxides are formed. For thick CoWP layers, the Cu diffusion to the surface is greatly reduced, and as a result, mainly Co oxides are formed. These results indicate that CoWP is not a good barrier for thermal oxidation, so high temperature exposure to oxidizing ambients must be minimized during processing of integrated circuits where CoWP is used instead of a dielectric barrier.

SESSION B7/O11: Joint Session: Fatique and Stress in Interconnect Metallization
Chairs: Paul Besser and Ralph Spolenak
Thursday Afternoon, March 31, 2005
Room 2004 (Moscone West)

1:30 PM *B7.1/O11.1
Thermal Fatigue in Cu Films. Cynthia A. Volkert[1,2], Reiner Moenig[1,2], Erica Lilleodden[1,2], Young Bae Park[3,2] and Guang Ping Zhang[4,2]; [1]Forschungszentrum Karlsruhe, Karlsruhe, Germany; [2]Max-Planck-Institut fuer Metallforschung, Stuttgart, Germany; [3]Andong National University, Andong, South Korea; [4]Shenyang National Laboratory for Materials Science, Shenyang, China.

Cyclic loading of metals can lead to the formation of damage and to failure even at loads that are well within the elastic range. In fact, the loading conditions present in the thin metal films and small metal structures used in many applications are often severe enough to lead to fatigue failure. In this study, TEM and in-situ SEM observations of thermal fatigue damage in sub-micron thick Cu films have been performed. As the crystal dimensions of the samples are decreased below 1 micron, by decreasing film thickness and grain size, a clear deviation from the characteristic fatigue damage of bulk metals is observed. The changes in dislocation structures, damage morphology, and failure lives are attributed to decreased dislocation motion and increased interface contributions. In particular, in samples with dimensions smaller than 300 nm, the damage morphology provides evidence for some surprising deformation mechanisms, such as twin dissolution and faceted grain growth. The implications of these observations on our fundamental understanding of deformation and on the reliability of small metal structures in microelectronic applications will be discussed.

2:00 PM B7.2/O11.2
TEM-Based Analysis of Defects Induced by AC Thermomechanical versus Microtensile Deformation in Aluminum Thin Films. Roy H. Geiss, Robert R. Keller, David T. Read and Yi-Wen Cheng; Materials Reliability, NIST, Boulder, Colorado.

Thin films of sputtered aluminum were deformed by two distinctly different experimental techniques. One experiment comprised of passing high electrical AC current density, 12.2 MA/cm^2 at 100 Hz, through 800 micron long X 3.3 micron wide and 0.5 micron thick patterned interconnect Al lines deposited on SiO_2/Si substrates. The other consisted of mechanical tensile deformation of a free standing Al line 50 micron long X 5 micron wide and 0.5 micron thick at a strain rate of about 10^{-4}/sec. In the electrical tests approximately 3X10^7 W/cm^2 of energy was deposited at 200 Hz resulting in cyclic Joule heating, which developed a total thermomechanical strain of about 0.3 % per cycle. The mechanical test showed a fracture strain of only 0.5 % but did display ductile chisel point fracture. In both experiments, certain grains exhibited large, greater than 30 degrees, rotation away from an initial <111> orientation toward <001>, based on EBSD measurements. TEM analysis of specimens from both experiments showed an unusually high density of prismatic dislocation loops. In the mechanically-tested samples, a high density of loops was seen in the chisel point fracture zone. While in cross sections of highly deformed regions of the electrical test specimens, very high densities, >10^{15}/cm^3, of small, <10nm diameter, prismatic loops were observed. In both cases the presence of a high density of prismatic loops shows that a very high density of vacancies was created in the deformation. On the other hand, in both cases the density of dislocations in the deformed areas was relatively low. These results suggest very high incidence of intersecting dislocations creating jogs and subsequently vacancies before exiting the sample. A discussion of this as well as other possible sources of the high vacancy concentration will be presented.

2:15 PM B7.3/O11.3

Employing Thin Film Failure to Form Templates for Nano-Electronics. Rainer Adelung, Mady Elbahri, Shiva Kuma Rudra, Abhijit Biswas, Sahid Jebril, Rainer Kunz, Sebastian Wille and Michael Scharnberg; Materials Science, CAU Kiel, Kiel, Germany.

Recently, we showed that thin film stress can be used to form well aligned and complex nanowire structures [1]. Within this approach we used stress to introduce cracks in a thin film. Subsequent vacuum deposition of metal leads the formation of a metal layer on the thin film and of metal nanowires in the cracks of the substrate. Removal of the thin film together with the excess metal cover finishes the nanowire fabrication on the substrate. As stress can be intentionally introduced by choosing an appropriate thin film geometry that leads to a stress concentration, the cracks and consequently the nanowires can be well aligned. Meanwhile, we have demonstrated how to form thousands of parallel aligned nanowires, x-and y-junctions or nanowires with macroscopic contacts for sensor applications, simply by applying fracture mechanics in thin films. Christiansen and Gösele called this approach "constructive destruction" in a comment in Nature Materials [2]. This gives a hint how to overcome some problems of the approach, arising from the limits of thin film fracture. A generalization of the fracture approach by being "more destructive" can overcome this limitations. This can be illustrated with an example: It is difficult to form pairs of parallel wires with a nanometer distance of the pair, but a micrometer separation between the individual pairs. Structures like this are useful for many contact applications including sensor arrays or field effect transistors. As well as thin film fracture, thin film delamination can be well controlled by fracture mechanics. Latest experiments show that the combination of both, fracture and delamination, forms an ideal shadow mask for vacuum deposition. Cracks with delaminated sides were used as templates for the deposition of pairs of parallel wires consisting out of different materials with only a few 10nm separation. This was done by first sputtering a metal under an angle of approx. 45° through the delaminated crack, which was used as a shadow mask. A second deposition of another metal is done afterwards under the opposite 45° with respect to the sample normal, having the crack located in the middle between both deposition sources. The angle, the delamination height and the crack width determine here the separation of the nanowire contacts. We present several examples which show how these mechanisms of mechanical failure of thin films can be turned into useful templates for various nanostructures. We will focus here on two standard thin film system, these are wet chemically deposited photo-resist and flash evaporated amorphous carbon. These examples are compared with finite element simulations. Moreover, we show how the delamination cracks can be also used as masks for the removal of material. Down to 20nm wide channels produced by ion beam sputtering are shown. [1] R. Adelung et al., Nature Materials, 3, 375, (2004). [2] S. Christansen and U. Gösele, Nature Materials, 3, 357, (2004).

2:30 PM B7.4/O11.4

Degradation of Fracture and Fatigue Properties of MEMS Structures under Cyclic Loading. Jong-jin Kim and Dongil Kwon; School of Materials Science and Engineering, Seoul National University, Seoul, South Korea.

The assessment of mechanical properties and reliability is essential to the development, commercialization and miniaturization of microelectromechanical systems (MEMS). The presence of flexural elements in MEMS applications like gyroscopes, optical switches or micromirrors raises concern about the effects of cyclic loading on material degradation or failure. Designing reliable MEMS devices thus requires knowledge of both the strength of such structural materials as silicon and nickel and also of its degradation with use. However, bulk material properties cannot be used directly for microscale systems because these properties deviate from bulk scaling laws when the characteristic dimensions become small. Thus, testing methods in the microscale range are of critical importance. In this study, the effects of cyclic loading on the fracture and fatigue of MEMS structures were investigated by combining resonance and microtensile methods. Microtensile-compatible resonating structures were designed and fabricated by micromachining that consisted of suspended beams, shuttle, combs and two kinds of electrodes with different areas. After these structures were electrostatically operated at their resonance mode by applying an AC voltage with a function generator, a two-step sacrificial-layer removal process was applied. Then static and dynamic loads much larger than electrostatic forces were applied by piezoelectric-driven microtensile techniques. Both tests were conducted in the same loading mode as the resonance test so as not to change failure mechanism, as is essential in accelerated life or degradation tests. Uniaxial stress-strain measurement results showed that tensile and fracture properties degraded with operation time at the resonance mode. Fatigue properties were measured by applying a pulse wave to a piezoelectric actuator: fatigue tests were conducted and fatigue lifetimes measured at various stress amplitudes. Stress-life (S-N) curves showed that fatigue lifetime and fatigue limit degraded with operation time at resonance mode in the same manner as tensile and fracture properties. These results suggest that fatigue damage accumulated during cyclic loading and increased with operation time. The dependencies of the measured properties on operation time were quantified, and fatigue damage was confirmed by failure analysis. Finally, the fatigue damage accumulation and materials degradation due to cyclic loading were discussed in terms of stress and materials.

2:45 PM B7.5/O11.5

Electrical and Mechanical Reliability of Cu Alloy Thin Film for Future Technology Node. Seol-Min Yi[1], Jeong-Uk An[1], Yong-Hak Huh[2], Young-Bae Park[3] and Young-Chang Joo[1]; [1]School of Materials Science and Engineering, Seoul National University, Seoul, South Korea; [2]Strength Evaluation Group, Korea Research Institute of Standards and Science, Deajeon, South Korea; [3]School of Materials Science & Engineering, Andong National University, Andong-si, Kyungsangbukdo, South Korea.

With miniaturization of advanced integrated circuits fabricated using the Cu damascene process, the higher current density is applied to and the thinner barrier layers are used in the lines therein. The high current density and the thin barrier layer may give rise to significant reliability problems, electromigration and drift of Cu into dielectric, respectively. Use of Cu alloy, as far as there is no significant increase in the electrical resistivity compared to that of pure Cu, has been suggested to address such problems. In this study, Mg and Ru were chosen as the alloying elements. Under oxidization ambient, Mg diffuses to the surface of a Cu(Mg) alloy thin film, on which a self-passivating Mg oxide layer is formed to block Cu drift into dielectric material and to enhance adhesion with a capping layer. Ru, which has the electrical resistivity lower than Ta(N) and negligible solid solubility with Cu, is expected not to increase resistivity of the corresponding Cu alloy. To characterize the effect of alloying elements on barrier performance, time-dependent dielectric breakdown (TDDB) under bias-temperature stress (BTS) tests were conducted using a metal-insulator-semiconductor (MIS) structure. Dependence of such effect on insulating material was also investigated. On the other hand, the effect of alloying elements on resistance to electromigration was quantitatively estimated by measurement of the adhesion between conducting metal and capping layers using the standard four point bending method. Since it is established well that the dominant path of electromigration in the Cu damascene structure is along the surface or interface, i.e. between Cu and a capping material, adhesion may be used as a effective measure to characterize the surface or interface. With the results of the microstructural and compositional analysis, the role of each alloy element in its alloy will be identified and discussed.

3:30 PM *B7.6/O11.6

Effect of Microstructure and Dielectric Materials on Stress-Induced Damages in Damascene Cu/Low-K Interconnects. Young-Chang Joo and Jong-Min Paik; Materials Sci. & Eng., Seoul National University, Seoul, South Korea.

The use of copper and low-k dielectrics led to various reliability concerns which were not issues in the interconnects with aluminum

and silicon oxide. For Cu/low-k interconnects, stress-voiding of Cu has been addressed to the main failure mechanism. Damascene Cu interconnects show significant differences in both microstructural and stress behavior compared to those of the Al interconnects patterned using the etching process. Large thermal stresses may build up during the successive thermal cycles due to the differences in the coefficients of thermal expansion (CTE) of the component materials. Other than thermal stresses, considerable amount of growth stress that is originated from grain growth may develop in damascene Cu interconnects as well. Furthermore, use of various low-k materials having lower elastic moduli and higher CTE make stress-related failures even more complicated to understand. In this study, the effect of microstructure and dielectric materials on stress-voiding was investigated using both experimental and theoretical approaches. The grain structure and the stress of damascene Cu lines having the width ranging from 0.1 to 2 μm were analyzed using TEM and x-ray diffraction. The contribution of the growth and thermal stress to the entire stress in the damascene structure were estimated by the finite element analysis (FEA). From this result, we developed a simulator based on FEA to assess the growth and the thermal stresses of a via-line structure. It was found that the stress state of a via-line structure varies dramatically depending not only on their geometries but also on the mechanical properties of dielectric materials. The corresponding failure is explained by the level of stress gradient as well as the stress itself. Also, the stress redistribution and relaxation induced by voiding was studied. Using our simulator and its results, the mechanisms of stress-induced failure in Cu/TEOS and Cu/low-k (having the high and the low CTE, respectively) are identified and discussed.

4:00 PM B7.7/O11.7

Comparison of Line Stress Predictions with Measured Electromigration Failure Times. Rao R. Morusupalli[1], William D. Nix[1], Jamshed R. Patel[1,2] and Arief S. Budiman[1]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL), Berkeley, California.

Reliability of todays interconnect lines in microelectronic devices is critical to product lifetime. The metal interconnects are carriers of large current densities and mechanical stresses, which can cause void formation or metal extrusion into the passivation leading to failure. The modeling and simulation of stress evolution caused by electromigration in interconnect lines and vias can provide a means for predicting the time to failure of the device. A tool was developed using MathCAD for simulation of electromigration-induced stress in VLSI interconnect structures using a model of electromigration induced stress. This model solves the equations governing atomic diffusion and stress evolution in one dimension. A numerical solution scheme has been implemented to calculate the atomic fluxes and the evolution of mechanical stress in interconnects. The effects of line geometries and overhangs, material properties and electromigration stress conditions have been included in the simulation. The tool has been used to simulate electromigration-induced stress in pure Cu interconnects and a comparison of line stress predictions with measured electromigration failure times is studied. Two basic limiting cases were studied to place some bounds on the results. For a lower bound estimate of the stress it was assumed that the interface can be treated like a grain boundary in Cu. For an upper bound estimate it was assumed that the interface can be treated like a free surface of Cu. Existing data from experimental samples with known structure geometries and electromigration failure times were used to compare the electromigration failure times with predicted stress build-up in the interconnect lines.

4:15 PM B7.8/O11.8

Stress-Induced Void Formation in Passivated Cu Film during Thermal Cycling and Isothermal Annealing. Dongwen Gan, Bin Li and Paul S. Ho; Laboratory for Interconnect and Packaging, University of Texas at Austin, Austin, Texas.

Stress voiding in Cu metallization is a critical yield and reliability concern. Stress-induced void formation in a passivated electroplating (EP) Cu film was studied during thermal cycling and isothermal annealing with the film stress measured using a bending beam technique. An optic microscope was used for the in-situ observation of the void formation and to determine the void density while SEM was employed to measure the void size and AFM for the topography analysis. In thermal cycling, voids were found to form under tensile stress and close under compressive stress, similar to the void formation observed by T.M.Shaw at al [1] in wide copper lines. The ramping rate, film stress as well as the thermal history were found important factors affecting the void formation in thermal cycling. During isothermal annealing, the void density and void size as functions of annealing temperature, and the void size as a function of time when the film was annealed at 250 degrees were measured. A critical temperature and stress were found for the void formation with the void density being proportional to the film stress, and an activation energy of 0.75eV was deduced for the void growth. Finite element analysis (FEA) models were set up to evaluate the local stress gradients in Cu films due to the mechanical anisotropy of Cu crystal, and that in a void vicinity as a function of void size, which was believed to account for the observed initial fast growth of a void. Mechanisms for the void formation are discussed. 1. T. M. Shaw, L. Gignac, X-H. Liu, R. R. Rosenberg, E. Levine, P. Mclaughlin, P-C. Wang, S. Greco, G. Biery, Stress Voiding in Wide Copper Lines, AIP Conference Proceedings, No612,2002, p.177-83.

4:30 PM B7.9/O11.9

Stress Generation in PECVD SiN Thin Films for Microelectronics Applications. Michael Belyansky[1], Nancy Klymko[1], Anita Madan[1], Anu Mallikarjunan[1], Ying Li[1], Ashima Chakravarti[1], Sadanand Deshpande[1], Anthony Domenicucci[1], Stephen Bedell[1], Edward Adams[1] and Sey-Ping Sun[2]; [1]IBM Microelectronics, Hopewell Junction, New York; [2]Advanced Micro Devices, Hopewell Junction, New York.

Stress generation in silicon is becoming one of the major knobs in boosting performance of the leading edge metal-oxide-semiconductor field effect transistor (MOSFET) technology. Substantial increase in device speed has been achieved by an application of highly stressed silicon nitride liner (SiN) films, which in turn produce an uniaxial stress in Si channel leading to electron and hole mobility enhancement. Thin SiN films (about 50nm) deposited by plasma enhanced chemical vapor deposition (PECVD) have been analyzed by a variety of analytical techniques including Fourier Transform Infrared Spectroscopy (FTIR), X-ray reflectivity (XRR), and Rutherford backscattering (RBS) to collect data on bonding, density and chemical composition respectively. Both tensile and compressive SiN films have been deposited and analyzed. Mechanisms of stress formation in SiN thin films are discussed. It has been found that amount of bonded hydrogen as detected by FTIR is higher for compressive films, and correlates with higher film density as determined by XRR. Both the density and number of interfaces in a film, characterized by XRR, affect the stress. Effect of deposition temperature and other process parameters on stress have been studied. Exposure of SiN films to elevated temperature after deposition lead to increase in tension and degradation in compressive stress. Process parameters, such as post-deposition treatments that result in modification of film structure and magnitude of tensile and compressive stress have been delineated.

SESSION B8: Poster Session
Chairs: Francesca Iacopi, Andrew McKerrow, Hermann Oppermann and Joost Vlassak
Thursday Evening, March 31, 2005
8:00 PM
Salons 8-15 (Marriott)

B8.1

A Novel Organic Low-k Film Deposited by Plasma-Enhanced Co-Polymerization. Nobutaka Kunimi[1], Jun Kawahara[1], Akinori Nakano[1], Keizo Kinoshita[1], Masashi Komatsu[1] and Takamaro Kikkawa[2,3]; [1]MIRAI-ASET, Tsukuba, Japan; [2]MIRAI-ASRC, AIST, Tsukuba, Japan; [3]RCNS, Hiroshima Univ., Higashi-Hiroshima, Japan.

A plasma-enhanced co-polymerization (PCP) technology has been developed, in which vaporized precursor monomers are activated by low electron density plasma and organic polymer films are deposited on a 300mm wafer. In this study, a new organic precursor is designed and synthesized to form polymer films having low dielectric constants by the PCP technology. In order to reduce the dielectric constant, a tricyclodecane (TCD) group is introduced as an organic precursor molecule because TCD is a large aliphatic hydrocarbon group, having a low dielectric constant. The new TCD precursor is liquid at the room temperature so that it has a sufficient saturated vapor pressure to be applicable to vapor phase deposition. The TCD film has dielectric constants less than 2.5, which could not be achieved by use of divinylsiloxane bisbenzocyclobutene (BCB) as a precursor. A solid ^{13}C-NMR spectrum of the 200°C-deposited film showed that TCD moiety in the precursor was included in the polymer without changing structure. Deposition temperature did not affect the dielectric constant of the TCD polymer films although FT-IR spectra showed a significant change on the intensity of the peaks due to hydrocarbon. On the other hand, the dielectric constant did not increase at 300°C but increased at 200°C and 400°C by acetylene co-polymerization. The unique behavior of the dielectric constant on the deposition temperature was studied by analyzing Raman spectra. It is revealed that the dielectric constant is strongly associated with sp^2 carbon content in the TCD-based polymer films. Consequently, the carbon structure is the most important factor that determines the dielectric constant of the organic low-k films.

B8.2

Pure-Silica-Zeolite Low-k Films from Nanoparticle Suspension. Zijian Li, Shaung Li, Christopher Lew and Yushan Yan; Chemical and Environmental Engineering, University of California, Riverside, Riverside, California.

Low dielectric constant (low-k) materials are needed to reduce signal delays, crosstalk noises and energy consumption in the next generation faster and more powerful microprocessors. The sub-90 nm technology is expected to be accomplished only with the use of a dielectric material with a k value lower than 2.4, but a manufacturable solution of such a low-k material is still unknown. Porous silicas including sol-gel silica and surfactant-templated mesoporous silica have been considered potential candidates for low-k materials and have been shown to be effective in lowering k values by taking advantage of the low dielectric constant of air (k=1). However, the trade-off between k value and mechanical strength raises concerns. Based on our previously reported in-situ MFI low-k films, we explored the possibility of extending the k value to below 2 by different methods without significantly lowering the mechanical strength. Low-k films prepared by spin coating from Pure-Silica-Zeolite(PSZ) MFI nanoparticle suspensions with high crystallinity have a k value around 1.6. We also report for the first time low-k films prepared from PSZ MEL nanoparticle suspensions. MEL small nanoparticles (~50 nm) with high yield (>50%) were obtained by using a two-stage synthesis method. The spin-on film with this yield has a k value of 1.8-2.0 and a low surface roughness (Ra=3.41 nm). High crystallinity MEL films have a k value around 1.5 and a good elastic modulus (~10 GPa).

B8.3

A New Methodology to Characterize and Model Cure Stress in Packaging Based on a Thermal Expansion - Cure Shrinkage Analogy. Hong Yu[1], S. G. Mhaisalkar[1] and E. H. Wong[2]; [1]School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; [2]MicroSystems, Modules & Components Lab, Institute of Microelectronics, Singapore, Singapore.

Thermosetting materials are widely used in electronic packaging. For the case of underfill materials used to reduce the thermal expansion mismatch and improve the reliability of flip chip interconnection, residual stress induced by the cure shrinkage as well as the thermal strain poses another reliability issue. However, for the case of electrically conductive adhesives used as an environmentally-friendly solution for interconnections by replacing lead-based solder balls, compressive stress is the main mechanism for conductivity establishment. Because of the development of mechanical properties and cure shrinkage during the curing process, the build-up of cure stress is fairly complex and often neglected. Moreover, to date, there are quite few reports on the simulation of the evolution of cure stress. In this paper, we report a novel method using a thermal expansion-cure shrinkage analogy to simulate the cure process using a commercial finite element analysis (FEA) software. A number of attempts have been reported for the characterization of cure shrinkage and mechanical property build up as the adhesive cures. A newly developed method based on thermomechanical analyzer (TMA) was used to measure the cure shrinkage of a non conductive adhesive (NCA) used in flip chip applications. It was found that the cure shrinkage increases linearly with degree of cure after gelation point. A new material constant namely coefficient of cure shrinkage (CCS) that characterizes the cure shrinkage as one of the material properties, which is independent of cure temperature and degree of cure is thus proposed. Degree of cure and CCS in the cure process are analogous to temperature and CTE in the thermal finite element analysis respectively. The implementation procedures using commercial FEA software are elaborated in this paper and an application to a NCA flip chip is described.

B8.4

Mesoporous Low Dielectric Poly(silsesquioxane) Thin Films Templated by Various Surfactants. Jingyu Hyeon-Lee, Hyeon-jin Shin, Jong-baek Seon, Hyun-dam Jeong and Jongmin Kim; Samsung Advanced Institute of Technology, Suwon, South Korea.

Mesoporous low dielectric poly(silsesquioxane) thin films have been fabricated by templating various surfactants such as cethyltrimethyl ammonium bromide or 4-octylphenol polyethoxylate in the silsesquioxane polymer matrix and their properties of the thin films characterized by electrical, mechanical and structural characterization. Depending on the types of the surfactants, mesoporous poly(silsesquioxane) thin films with different mesostructures and porosities have been formed via self-assembly and calcination induced structural transformation. The dielectric constant (k) of the films depended on the content or porosity of the surfactants. The dielectric constants of ca. 1.9-2.1 were obtained for the films with relative porosities of about 30-40 vol. % to the polymer matrix itself. The elastic modulus of the films showed a dependency on the type, content of the surfactants and was ca. 6 GPa with the k value of ca. 2.30.

B8.5

Spin-on Dielectric Materials for High Aspect Ratio Gap Fill for 70 nm Node and Beyond. Wei Chen, Sheng Wang, B. K. Hwang, Ather Ashraf and J. K. Lee; Dow Corning Corporation, Midland, Michigan.

As the IC design rules continue to get smaller, trench dimensions are getting narrower and trench aspect ratios are increased. Traditionally, chemical vapor deposition (CVD) oxides are the standard materials for the gap filling applications, including shallow trench isolation (STI) and pre-metal dielectric (PMD) trenches. However, for the technology nodes 70 nm and beyond, the CVD technologies including HDPCVD are facing various challenges, such as void formation in the high aspect ratio gaps. Although new CVD technology is evolving, the throughput could still be a major issue. Alternatively, spin-on dielectric (SOD) materials provide feasible pathways for the high aspect ratio gap filling with the potentials of easy process and high throughput. We have investigated a number of hydrogen silsesquioxane and methyl silsesquioxane materials for gap filling. The trench gaps range from 20 to 200 nm in width with aspect ratios varying from 1 to 7. Generally, the SOD materials can achieve good gap fills, even in the 20 nm gap with the aspect ratio of 7. While a decent gap fill by a SOD material is relatively easy to accomplish, the greatest challenge remains in material densification in a narrow trench. The narrow opening in such a trench limits the material flow while the SOD material is shrinking during the cure. Typically, the bottom of a gap is not as dense as the top part. Wet etch selectivity serves as a screening method for trench densification. Different processing and cure conditions are used to increase material densification in the trenches. We will discuss the effects of various thermal cure schemes, plasma cure, and alternative cure methods of SOD materials in these nano-scale trenches. While the SOD materials can be cross-linked in the gaps, different cure schemes significantly impact wet etch selectivity.

B8.6

Annealing-Induced Adhesion Enhancement at Cu-SiO_2 Interfaces Modified with Organosilane Nanolayers. Darshan D. Gandhi, P. G. Ganesan, A. P. Singh and G. Ramanath; Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York.

Isolating and tailoring the structural properties of metal-dielectric interfaces is a critical challenge for realizing high performance interconnect wiring in nanodevices. We have recently demonstrated the potential of organosilane and polyelectrolyte nanolayers to inhibit Cu diffusion and enhance adhesion at Cu-SiO_2 interfaces[1,2]. The barrier properties of 0.7 to 3.5-nm-thick molecular layers are superior compared to the sputter-deposited barriers of Ta of similar thickness. However, little is known regarding the thermal stability of structures modified with molecular layers and the effects of annealing on properties. Both are important questions to be addressed to assess the feasibility and facilitate the integration of molecular layers with device fabrication processes, and porous low-k dielectrics. Here we report that 3-Mercaptopropyltrimethoxysilane (MPTMS) molecular layers in Cu/MPTMS/SiO_2 structures not only withstand temperatures near 400°C, but also result in a remarkable ~5-fold increase in debond energy (measured by 4-point bending) compared to debond energies measured for untreated interfaces. The effects of pristine and sulfonated MPTMS nanolayers and the nature of the siloxane bond on the adhesion enhancement mechanism are revealed by X-ray photoelectron spectroscopy of fracture surfaces. Thiol-terminated layers result in a factor-of-3 increase in debond energy at room temperature, followed by a 60% decrease upon annealing <400°C. Sulfonated nanolayers show negligible effect on the debond energy in this temperature range. Annealing >400°C, however, results in monotonic debonding increase reaching up to ~15 J/m^2, which is a ~factor-of-5$greaterthanthatmeasuredforuntreatedCu-SiO_2$ interfaces. Cu fracture surfaces showing S 2p, Si 2p and O 1s signatures corresponding to thiol and silanes indicate debonding at the MPTMS-SiO_2 interface. Cu 2p and O 1s spectra reveal Cu-SO_x bond formation, which increase above 400°C. Si 2p and O 1s spectra showed an increased siloxane bond density in samples annealed to >400°C, suggesting siloxane bond stabilization through irreversible dehydration of silanol groups. This was experimentally verified by kinetics measurements of the dehydration process using infrared spectroscopy. Thus, strengthening of bonding interactions at both Cu-MPTMS and MPTMS-SiO_2 interfaces contribute to enhanced interfacial adhesion. Our results showing enhanced adhesion and thermal stability of molecular layers at elevated temperatures is promising for integrating organic nanolayers into future nanodevices.
1 P.G. Ganesan, J. Gamba, A. Ellis, R.S. Kane, and G. Ramanath, Applied Physics Letters **83** (16), 3302-3305, (2003). 2 P. G. Ganesan, A. P. Singh, and G. Ramanath, Applied Physics Letters **85** (4), 579-81, (2004).

B8.7
Post-Etch Measurement of Via Bottom Residues.
Cecilia C. Martner, Peter Borden, Edgar Genio, Michael Wood, Jianshe Tang and Philip Fulmer; AMAT, Santa Clara, California.

One of the most challenging aspects of Cu damascene fabrication is obtaining uniformly clear via hole bottoms following etch and clean. Residues and excess CuOx growth are common sources of high resistance and electro migration failure. Today, there is no effective way to identify these residues before electrical test. High aspect ratio SEM lacks resolution capability, and TEM preparation is costly and lengthy. Electrical test necessitates complete fabrication of structures, requiring long cycle time and convolving results with variation from the wafer processing steps after etch and clean. We describe a method of characterizing via bottoms in dense 0.12 mm via structures that have been etched and cleaned prior to barrier/seed deposition. This technique, based on a two-laser power absorption method, is fast (3-4 min per test structure), non destructive and has a 2 mm spot size, enabling in line local and cross-wafer uniformity measurements for process development and process monitoring. The results reported in this paper focus on the detection of thin residuals and oxide films at the bottom of the vias. We present studies of via conditioning as a function of time after wet clean processing, showing sensitivity to CuOx growth at the bottom of the vias (M1 metal exposed to ambient). This paper also provides experimental results for different post-etch clean process parameters, including both wet and dry processing, showing how metrology shortens the process optimization cycle time to deliver improved uniformity and performance of the post-etch clean process.

B8.8
Pressure Dependent Parylene-N Pore Sealant Penetration in Porous Low-k Dielectrics. Jasbir S. Juneja[1], Gregory A. Ten Eyck[1], Hassa Bakhru[2] and Toh-Ming Lu[1]; [1]Center of Integrated Electronics, Rensselaer Polytechnic Institute, Troy, New York; [2]Department of Physics, SUNY, Albany, New York.

Low-k dielectric materials are needed to reduce interconnect delay in integrated circuits. Introducing porosity is considered to be a possible solution for continuous scaling of low-k dielectrics. It is also desirable to use Chemical Vapor Deposition (CVD) or Atomic Layer Deposition (ALD) techniques to deposit a metallic layer on top of the porous dielectrics. However, direct metallization on porous dielectrics results in penetration of gaseous CVD or ALD precursor into the pores and the subsequent metal deposition in the dielectric itself. A thin layer of chemical vapor deposited Parylene-N has been shown to prevent CVD precursor penetration in porous ultra-low k dielectric methyl silsesquioxane (MSQ).[1] It was also shown that Parylene-N itself penetrates into porous MSQ. The depth profile of Parylene-N in porous MSQ can be obtained using the Nuclear Reaction Analysis (NRA) of ^{12}C, since Parylene-N is $[C_8H_8]_n$. ^{12}C exhibits a strong (α,α) elastic scattering resonance in the energy region ~4.3MeV. At this energy the cross section is more than 2 orders higher than the Rutherford cross section and therefore small changes in Carbon concentration can be detected. This paper presents the deposition pressure dependence of the penetration of Parylene-N in porous MSQ. The experimentally measured effective dielectric constant after pore sealing is compared to the one calculated using the NRA data of Parylene-N penetration. Higher deposition pressure results in lower penetration of Parylene-N into porous MSQ, and hence least change in effective dielectric constant, since the deposition rate is higher at higher pressures and the pores seal off quickly. A higher deposition rate of Parylene-N can also be achieved by adding carrier gas. Parylene-N penetration in porous MSQ will be presented for the case where the deposition was done with an Argon carrier gas used to raise the system pressure. [1]Christopher Jezewski, W.A. Lanford, C. J. Wiegand, Jay J. Senkevich, T.-M. Lu, "Effective pore sealing of ultralow-k dielectrics", Semiconductor International, v 27, n 5, 2004, 56-59

B8.9
The Effect of Film Composition on the Properties of PECVD Low-k a-SiCO:H Films. Byung Keun Hwang, M. Tzou, A. Ashraf and B. Nguyen; Dow Corning Corporation, Midland, Michigan.

Amorphous silicon oxycarbide (a-SiCO:H) films with dielectric constants ranging between 3.0 to 2.5 were grown on a conventional plasma-enhanced chemical vapor deposition (PECVD) reactor using various organosilanes as CVD precursors. By changing CVD precursors and the conditions of PECVD processes, the composition of a-SiCO:H films and, as a result, the thin film properties of resulting films could be tailored. Especially, in this study, as an alternative to adding porogens into films during process, the C/Si ratio in the film was manipulated in a way to change the dielectric constant of films as well as other film properties. The films grown with different CVD precursors and PECVD processes were characterized by Fourier transform infrared (FTIR), Rutherford backscattering (RBS), Hysitron triboindentor, stud-pull test, modified edge lift test (m-ELT) and electrical measurements on metal-insulator-silicon (MIS) structures. With new CVD precursors and control of process conditions, it is possible to get a-SiCO:H films with k of 3.0 to 2.5 and modulus of 16 to 3 GPa without any post treatment. We found that by using different CVD precursors we could get a-SiCO:H films which had the same k of 2.8, but with modulus values ranging from 4 to 13 GPa. Also the carbon enriched a-SiCO:H films showed improved toughness and adhesion properties. The results imply that the selection of the right CVD precursor for low-k application would be very important to develop a robust PECVD low-k film. In this paper we will discuss the effect of composition and bonding structures of a-SiCO:H films grown with different CVD precursors on the thin film properties.

B8.10
New Carbon-Bridged Hybrid Polymer for low-k Materials. Bum-gyu Choi, Byung Ro Kim, Myung-sun Moon, Jungwon Kang, Gwigwon Kang and Min-Jin Ko; LG Chem, Daejeon, South Korea.

Reducing interline capacitance and line resistance is required to minimize RC delays, reduce power consumption and crosstalk below 100nm node technology. For this purpose, various inorganic- and organic polymers have been tested to reduce dielectric constants in parallel with the use of copper as metal line. Lowering the dielectric constants, in particular, causes the detrimental effect on mechanical properties, and then leads to film damage and/or delamination during chemical-mechanical planarization (CMP) or repeated thermal cure cycles. To overcome this issue, new carbon-bridged hybrid materials synthesized by organometallic silane precursors and the sol-gel reaction are proposed. In this work, we have developed new organic-inorganic hybrid low-k dielectrics with linear or cyclic carbon bridged structures. The different bridged carbon structures were formed by a controlled reaction. Solid-state 13C CP MAS NMR and 29Si MAS NMR analyses were conducted for the structural characterization of new hybrid low-k dielectric. The mechanical and dielectric properties of these hybrid materials were characterized using nanoindentation with continuous stiffness measurement and Al dot MIM techniques. The results indicate that these organic-inorganic hybrid materials are very promising polymers for low-k dielectrics that have low dielectric constants with high thermal and mechanical properties. It has been also demonstrated that electrical and mechanical properties of the hybrid films can be tailored by copolymerization with PMSSQ and through the introduction of porogen.

B8.11
Development of Hermetic Oxide Films For Low k Pore Sealing. Kang Sub Yim, Vu Nguyen, B. H. Kim, Alex Demos, Girish Dixit, Derek Witty and Hichem MSaad; Applied Materials, Santa Clara, California.

Porous low k materials are being widely studied using both CVD and spin-on processes. The incorporation of nano-porosity into films is the most common approach to further reductions in k value and thus RC delay. The porous low-k materials, however, are known to have several integration issues such as gas absorption, metal diffusion, and k increase during subsequent etching/ashing/cleaning processes. It is known that the surface sealing of porous low-k materials prior to barrier deposition is one of the solutions to avoid any diffusion or discontinuity of the metal barrier layer. New hermetic oxide films are developed as pore sealing layers using organosilane-type precursors deposited by PECVD technology. An approach to make denser films with good step coverage was used in this work. Oxide films with higher density showed more compressive stress and lower wet etch rate. Hermeticity was measured by monitoring the stress change after 85oC, 85% humidity (85/85) moisture absorption test. Three different films were tested for hermeticity. Oxide films with low density showed a dramatic stress change at all thickness ranges after 85/85 humidity cooking test, indicating significant moisture uptake; while the stress change was very minimal for films with a higher density. For highly dense films, it was found that 100$\AA$ thick oxide layers were equally effective as sealing layers. A similar hermeticity trend was observed in other physical properties such as thickness, RI, and dielectric constant. This hermeticity trend in various oxide films could be explained by moisture uptake during 85/85 test. This result indicates that denser films are hermetic and can resist moisture absorption/uptake, suggesting that they can be used as capping layers to prevent possible damage to the underlayer film when exposed to wet chemistries. FTIR analysis illustrates that non-hermetic oxide films which are less dense have Si-O peak shifts to a lower wave number, inferring that the Si-O angle is more constrained. From these results, it appears that hermeticity is related to the oxide structure and film density. For major applications of these hermetic oxide films such as pore sealing and spacer layers, the conformal deposition of thin oxide is very important. TEM pictures of thin hermetic oxide

films confirm that the hermetic oxide layers can be deposited with excellent conformality.

B8.12

The Effect of Methylating Treatments on the Dielectric Reliability of Low-k/Cu Structures. Swarnal Borthakur[1,2], Sri Satyanarayana[1], Andreas Knorr[1,3] and Paul S. Ho[2]; [1]Sematech, Austin, Texas; [2]The University of Texas at Austin, Austin, Texas; [3]Infineon Technologies, Munich, Germany.

As scaling approaches nanometer levels, the RC delay of interconnects has become a dominant factor in determining the total delay. Etching, ashing and cleaning processes damage the dielectric [1]. In general, porous low-k materials are more prone to damage compared to dense ILD. This damage is carried forward into subsequent processing steps and ultimately leads to higher effective dielectric constant [2]. The damage also increases the leakage current through the inter-level dielectric (ILD) and compromises the reliability of the interconnect structures. In this paper we investigate different chemicals that can be used to repair the damage to the dielectric and recover the k-value. The same chemicals could also act as a pore sealant that will prevent copper penetration into the ILD and improve the reliability. The chemicals used in this study are organic compounds with methyl groups because the ILD is a methyl silsesquioxane (MSQ) material [3]. We will present physical (TEM/EELS, AFM, FTIR) and electrical (k-value, leakage current, ramp-voltage-breakdown and TDDB) characteristics of single damascene structures (0.13μm on 300mm) with different chemical post-ash treatments. The RC delays will be compared among different treatments. The breakdown field is determined from ramp-voltage-breakdown tests performed on comb/comb test structures. The breakdown field is then compared over a wide range of pitch. In addition, annealing effects are being studied. Dielectric reliability characteristics will be compared. The structures were stressed at RT and high fields (>3.0 MV/cm). The effectiveness of the methylating treatment is determined by comparing the breakdown characteristics. The high field and RT test conditions may cause breakdown to occur due to barrier lowering (charge injection) at the interfaces as well as molecular degradation of the ILD. Further details will be provided in the paper. References: [1] L. Peters, Semiconductor International, Oct 1st 2002. [2] P.G. Clark et al., Semiconductor International, Aug 1st 2003. [3] Y. S. Mor et al., J. Vac. Sci. Technol. B 20(4), 2002.

B8.13

Standard Porosimetry. Yury Volfkovich, Igor Blinov and Alexander Sakars; Porotech Ltd., Vaughan, Ontario, Canada.

The widely known Method of Mercury Porosimetry (MMP) has several substantial disadvantages, for example, the necessity to apply high pressures of mercury, which can lead to destruction of samples and to a distortion of the porosimetric curves (porograms). Other drawbacks MMP are: distortion of the results owing to amalgamation of most metals, different values of the mercury wetting angle for different materials, toxicity of mercury, etc. We developed a new method - the Method of Standard Porosimetry (MSP) and Automated Standard Porosimeter (ASP). MSP and ASP have non of these disadvantages and give the possibility of measurements in a widest range of pore sizes ($\sim$ from 0.3 to 300000 nm) for any materials including soft or frail materials or amalgamating materials. MSP is based on the laws of capillary equilibrium. If two (or more) porous bodies are in contact with one another and partially filled with a wetting liquid (hydrocarbons, water etc.) are in the state of capillary equilibrium then the values of the capillary pressure P of the liquid in these bodies are equal. The capillary pressure can be represented by the Laplace equation If for one of the porous bodies (the standard sample) the pore size distribution is known, then by determining an equilibrium dependence of liquid content for a test sample on liquid content for standard sample, the pore size distribution for the test sample can be calculated. The amount of liquid in the samples is determined by weighing. The standards and test samples are preliminarily (under vacuum) filled with a liquid. The stack of porous samples is assembled in a special clamping device in which the samples are tightly pressed to each other. From this assembly a small portion of the liquid is evaporated by vacuum treatment or by a flow of dry inert gas. The ASP includes a automatic manipulator for the assembling and disassembling of the stack of samples and for the transfer of the samples to the balance. Any porous and dispersed bodies can be investigated by MSP and ASP, for example, electrodes, membranes, separators, filters, catalysts, carbon nano-tubes, adsorbents, ceramics, metallic ceramics, textiles, pharmaceuticals, construction materials, polymers, geological strata, etc. MSP/ASP allows for determination of a variety of information about porous and dispersed bodies: pore volume and specific surface distribution in terms of pore radii, specific surface area, information about a shape (corrugation) of pores, liquid distributions in terms of values of its free binding energy and capillary pressure with the testing material, sorption isotherms, differential characteristics of swelling, contact angle and its dependence on pore radii, characteristics of hydrophobic-hydrophilic properties, etc.

B8.14

Capacitance Measurement Technique for Determining the Out-of-Plane Coefficient of Thermal Expansion for Low-k Dielectrics. Swarnal Borthakur[1,2], Andreas Knorr[1,3], Paul S. Ho[2] and Wen-Li Wu[4]; [1]Sematech, Austin, Texas; [2]The University of Texas at Austin, Austin, Texas; [3]Infineon Technologies, Munich, Germany; [4]NIST, Gaithersburg, Maryland.

As scaling approaches nanometer levels, the RC delay of interconnects has become a dominant factor in determining the total delay. The low-k dielectrics that are being investigated for reducing the capacitance are based on carbon-doped oxide or are organic materials. A major concern in the integration of low-k materials is the thermal stress generated in the structure due to the thermal expansion mismatch between the low-k material and its adjacent surroundings. The out-of-plane coefficient of thermal expansion (CTE) can be determined by X-ray reflectivity technique (XRR) [1]. In this paper we present a characterization technique for determining the out-of-plane CTE of low-k materials from capacitance measurements. This technique relies on accurate capacitance measurements over temperature in a N_2 environment. It is relatively easy to perform and simpler than the XRR technique. The test structure is an MIM capacitor with aluminum dots as top electrode and highly doped low-ρ silicon as the substrate. Capacitance is measured over a wide range of temperature (25-300°C) and measurements are made in a N_2 environment. By combining the equations for a parallel plate capacitor and coefficient of thermal expansion we get the equation [2] [3], $\alpha = -\Delta C/C\Delta T$ In this equation, ΔC is the change in capacitance; ΔT is the temperature range and α is the coefficient of thermal expansion (CTE). This equation does neglect the temperature dependency for the material's k value. We will discuss measurement corrections and instrumental limitations and present data for both carbon-doped films and organic films. The CTE values obtained by this technique will be compared with those obtained from XRR technique. The dependence of the dielectric constant on temperature and its effect on the calculated CTE values will be discussed. References: [1] Wen-Li Wu and Huey-Chiang Liou, Thin Solid Films, 312 (1998), 73-77. [2] G. D. Sao and H. V. Tiwary, L. Appl. Phys. 53(4), April 1982. [3] H. M. Tong et al., Rev. Sci. Instrum. 62(2), Feb 1991.

B8.15

Determination of Elastic Modulus and Yield Stress of Ultra-thin Cu and Low-k Films Using Spherical Nanoindentation Measurement. Satoshi Shimizu, Nobuo Kojima and Jiping Ye; Reserch Department, Nissan Arc, Ltd., Yokosuka, Japan.

Quantitative nanometer-scale estimations of mechanical properties are important in the development of multilevel interconnect technology for ultra-large-scale integrated circuits. Recently, a convenient nanoindentation measurement technique based on Oliver's method has been widely used for evaluating the hardness and elastic modulus of thin films. This technique has some limitations in estimating elastic properties in the elastic deformation range and yield stress due to plastic deformation. Although these properties are indispensable to determine the mechanical strength of multilevel interconnect structures, up to now, for example, macro-meter-scale mechanical data obtained from bulk materials have still been applied in computer simulations for estimating stress distributions on a nanometer scale. In our recent studies, we have successfully developed a spherical nanoindentation method for determining the yield stress of tribofilms on a nanometer scale [1]. In this work, we applied this spherical nanoindentation method to evaluate the elastic modulus in the elastic deformation range and the yield stress of ultra-thin Cu and low-k films. A spherical indenter with a radius of 1 μm was chosen because this shape is conducive to mechanical analysis in terms of the Hertz contact theory and the Tresca yield criterion. Measurement effectiveness was examined by using two differently oriented single crystals Cu (111) and Cu (100). The Cu (111) plane exhibited initial plastic deformation in the load-depth curve at 9.5 μN and the Cu (100) plane displayed it at 7 μN. Under the Tresca yield criterion with a Poisson's ratio of 0.3 and a tip radius of 1 μm, the Cu (111) plane was estimated to have elastic modulus of Er = 91GPa and shearing yield stress of σy = 340MPa, both of which were smaller than the values of Er = 68GPa and σy = 290MPa estimated for the Cu (100) plane. This anisotropic nature of these mechanical properties, which were never seen on a macro-meter scale, agreed with metallurgical considerations of an active f.c.c. slip system. This method was also applied to Cu and low-k films. It was confirmed that the Cu thin films possessed anisotropic elastic modulus and shearing yield stress due to the different crystallographic orientations present in the film plane. By using an indenter with a small radius of less than 150 nm, this method makes it possible to evaluate the elastic modulus and yield stress of 20-nm-thick ultra-thin films. [1] Jiping Ye, Makoto Kano and

Yoshiteru Yasuda, Tribology Letters, 13 (2002) p. 41.

B8.16
Property Assessment of Some Low-k Films on Silicon. Martina Damayanti[1,2], Johnny Widodo[2], Thirumany Sritharan[1], Subodh Gautam Mhaisalkar[1], Wei Lu[2], Zhenghao Gan[1], Kai Yang Zeng[3] and Liang Choo Hsia[2]; [1]Materials Technology, Nanyang Technological University, Singapore, Singapore; [2]Technology and Development Dept, Chartered Semiconductor Manufacturing Ltd., Singapore, Singapore; [3]Institute of Materials Research and Engineering, Singapore, Singapore.

Chemical vapour deposited (CVD) low-k films using tri-methyl-silane (3MS) and tetra-methyl cyclo-tetra-siloxanes (TMCTS) precursors were studied. A four-point bend test (4PBT) was performed to assess the adhesion property of the low-k films to Si substrates and the results were compared with that of simpler method, nanoscratch test (NST), as a quality control tool despite its drawbacks. Adhesion energy, Gc, of the low-k/Si interface as measured by 4PBT and critical scratch load, Pc, as obtained by NST display a linear relationship with hardness and modulus of the low-k film. The lowering of Gc as the hardness of the film decreases can be explained by the effects of the C introduction into the Si-O networks found in these films. Lower Carbon content for higher hardness films is thought to cause them to be more silica-like and thus exhibit better adhesion with the Si substrate. Two failure modes were observed for specimens under 4PBT. On one hand, films with low hardness (<5 GPa) exhibit low Gc (<10 J/m2) with an adhesive separation of low-k from the Si substrate. On the other hand, films of high hardness (>5 GPa) display interfacial energies in excess of 10 J/m2 with delamination of epoxy from the Si substrate, thus indicating excellent adhesion between the low-k films and Si substrate. Under 4PBT, initially the load increases linearly as the specimen deforms elastically. At some point, the load decreases abruptly which signifies the point at which the vertical crack initiated by the notch begins to propagate through the Si. When it reaches an interface, it might be either deflected to propagate along the interface or continue through the next material in its vertical path. The crack takes the path that has the least energy dissipation. Thus, the crack path would be determined by the adhesion at the interface and the toughness of the material ahead. For the low hardness films good correlation exists between Pc and Gc. However the two data points of the high hardness films that gave the two highest Pc and Gc values do not lie on the correlation line drawn for the low hardness film data points due to different factors governing the failure in both tests and a change in the 4PBT failure mechanism. Therefore correlating results obtained by the 4PBT to other empirical tests must be done with caution.

B8.17
Mechanical Strength Enhancement in Porous Silica Films by TMCTS Treatment. Nobutoshi Fujii[1], Takahiro Nakayama[1], Takenobu Yoshino[2], Nobuhiro Hata[2], Yutaka Seino[2], Yuko Takasu[2] and Takamaro Kikkawa[2,3]; [1]MIRAI-ASET, Tsukuba, Japan; [2]MIRAI-ASRC-AIST, Tsukuba, Japan; [3]RCNS, Hiroshima Univ., Higashi-Hiroshima, Japan.

In order to adopt porous silica films to interlayer dielectrics (ILD), mechanical strength is an issue in the chemical mechanical polishing process. We have reported that 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS) vapor treatment significantly enhanced the mechanical strength of porous silica films without increasing the dielectric constant k. In this study, it is demonstrated that the enhanced polymerization of TMCTS molecules can be achieved also by Cs doping in porous silica. It is known that sodium can enhance the polymerization reaction of TMCTS molecules on the pore wall surfaces of porous silica, leading to the enhancement of the mechanical strength. However, sodium is not acceptable for semiconductor manufacturing. In this respect, the sixth periodic elements could be candidates for enhancing the polymerization reaction of TMCTS. Owning to its large mass number and ionic radius, cesium (Cs) is a candidate as a dopant in porous silica because Cs is stable enough in the SiO_2 network at normal device operating temperatures. [1] Indeed, by doping of 500 ppm Cs in porous silica, the mechanical strength of the film with a dielectric constant of k=2.0 was improved from 4 GPa to 7.2 GPa. The mechanical strength enhancement was considered to be caused by the increase of Si-O-Si bonds on pore wall surfaces in the Cs doped porous silica film, as confirmed by the FT-IR spectra. The Cs-doped porous silica film has higher mechanical strength and lower dielectric constant than non-doped porous silica film because higher mechanical reinforcement and hydrophobicity were achieved simultaneously by the enhanced polymerization of TMCTS. There are no significant differences in the electrical properties, such as leakage current density and breakdown electric field. [1] B. J. Fishbein and James D. Plummer, Appl. Phys. Lett. 50, (1987), 1200-1202.

B8.18
Application of Nanoindentation to Characterize Fracture in ILD Films used in the BEOL. Eva Erika Simonyi, Eric Liniger, Michael Lane, Christos D. Dimitrakopoulos and Christy S. Tyberg; IBM TJ Watson RC, Yorktown Heights, New York.

It is of importance to measure the so called critical film thickness, above which spontaneous cracking could occur. Nanoindentation method is presented as a tool to estimate the critical film thickness for ILD films used in the BEOL. This allows to calculate cohesive energies and fracture toughness of the films. Several materials were investigated using nanoindentation combined with AFM imaging. The results were compared to data acquired by four point bend methods.

B8.19
The Role of Friction and Loading Parameters in Four-Point Bend Adhesion Measurements. David M. Gage[1], Kyunghoon Kim[2], Christopher S. Litteken[1] and Reinhold H. Dauskardt[1]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Mechanical Engineering, Stanford University, Stanford, California.

The 4-point bend method has become a widely established technique to quantitatively examine the cohesive and adhesive fracture energies of thin film structures. In the present work we report on the effects of loading point friction, applied loading geometry and loading rate on four-point bend fracture measurements. To date, these effects together with other salient loading parameters have received little attention and have not been systematically studied. Technologically relevant interconnect thin film structures containing either carbon doped oxide or thermal oxide low-k dielectrics and selected barrier layers were prepared and tested in four-point bending to determine the dependence of the measured fracture energy, G_c, on loading parameters and specimen geometry including the loading rate, load point separation, and specimen surface condition. Fracture energy measurements were found to be sensitive to applied loading geometry and displacement rate, particularly for specimens with G_c values above 5 J/m^2. We show that this behavior is due to a combination of Coulomb friction and stress corrosion effects. Good practice testing guidelines are suggested to improve the accuracy and precision of four-point bend measurements.

B8.20
Abstract Withdrawn

B8.21
Rapid Characterization of the Electrical and Micro-Structural Properties of Molybdenum-Tungsten Electrodes using a Combinatorial Thin Film Sputtering Technique. Seung-Ik Jun[1], Timothy E. McKnight[2], Anatoli V. Melechko[2,1], Michael L. Simpson[1,2] and Philip D. Rack[1]; [1]Materials Science and Engineering, The University of Tennessee, Knoxville, Tennessee; [2]Molecular Scale Engineering and Nanoscale Technologies Research Group, Oak Ridge National Laboratory, Oak Ridge, Tennessee.

Molybdenum-tungsten (MoW) alloys have great potential uses for high temperature and low resistivity electrodes. These alloys are particularly useful in inverted metal-oxide-semiconductor (MOS) devices where a etch taper angle is desirable for device reliability. In order to investigate the electrical characteristics and micro-structural properties of MoW as a function of the binary composition, a combinatorial RF magnetron sputter deposition technique was employed. Additionally, we investigated the effects of substrate bias and temperature. The electrical resistivity of MoW thin films deposited at room temperature and without bias followed the typical Nordheim's rule as a function of composition. The resistivity increases with tungsten fraction and has a maximum value around 0.5 atomic fraction of tungsten. In this sputtering condition, a metastable β-W phase was identified, which results in a significantly higher resistivity due to the lattice mismatch between stable α-W and metastable β-W. MoW films deposited at higher temperature (250 °C) also followed Nordheim's rule as a function of composition, however it didn't contain the metastable β-W phase and consequently had a lower resistivity than the room temperature deposition. MoW thin films deposited with substrate bias had a considerably lower resistivity over the overall composition range and its resistivity as a function of composition obeyed the rule of mixtures. The β-W is not present in bias sputtered samples even room temperature as the tungsten phase was entirely stable α-W. Additionally, unlike bulk molybdenum and tungsten, biased tungsten-rich films had higher resistivity than biased molybdenum-rich films. This phenomenon was attributed to the fact that the dislocation resistivity of tungsten is two orders of magnitude higher than that of molybdenum. The results from high resolution scanning electron microscopy revealed that a denser micro-structure was realized in the biased films, which correlated to the significantly lower electrical resistivity of the films. Finally, MoW thin films were found to be thermally stable with plasma enhanced chemical vapor deposited silicon dioxide up to 700 °C.

B8.22

Conducting Ruthenium Oxide Nano-Layers by UV-Ozone Oxidation. Vaishali Ukirde[1], Changduk Lim[1], Oliver Chyan[2] and Mohamed El Bouanani[1]; [1]Materials Science, University of North Texas, Denton, Texas; [2]Chemistry, University Of North Texas, Denton, Texas.

Ruthenium and its oxides and nitrides are potential candidates for number of advanced applications in Silicon based semiconductor technology such as metal-based gate electrodes and diffusion barriers for copper interconnects. This is due to their good thermal stability, low resistivity, suitable work function and diffusion barrier properties. Physico-chemical and electrical properties of Ru oxides are intimately dependent on the oxide preparation method mainly due to the resulting microstructure, oxidation state and impurities/contaminants. 5 to 7 nm Ru films were deposited on Si and SiO2 substrates by DC magnetron sputtering in Ar atmosphere. The films were then exposed to UV/Ozone radiation and oxygen at room temperature for a duration ranging from 15 min to 60 min. In-situ X-ray photoelectron spectroscopy (XPS) is used to investigate Ru oxidation rate and the bonding environment. A comparison with Ru oxide prepared via reactive DC sputtering in an Ar/O2 mixture will be presented.

B8.23

Advanced Al Damascene Process for Fine Trench under 70nm Design Rule. Sung Ho Han, Kyung-in Choi, Serah Yun, Jeong Heon Park, Sang Woo Lee, GilHeyun Choi, Sung Tae Kim, U-In Chung and Joo-Tae Moon; Samsung Electronic Co. Ltd., Yongin-City, Kyungki-Do, South Korea.

As interconnect geometry shrinks beyond 100nm technology, Tungsten bit-line could be problematic due to high line resistance. In order to reduce the line resistance, the stack height needs to be increased, while it causes an increase in parasitic capacitance. The parasitic capacitance reduction becomes more important in high-speed device such as Nand-Flash, high speed SRAM etc. Thus, Al interconnect can effectively reduce line resistance, but Al RIE has a difficulty in pattering for fine pitch, like beyond 70nm design rule. In this paper, the filling characteristic of the new CVD-Al metallization scheme is mainly studied in single damascene pattern. Trench patterns with beyond 70nm in ground rule were fabricated for single damascene process. Combination of CVD TiN with excellent step coverage and metal rich PVD TiN is used as under layer for CVD-Al deposition. CVD-Al is deposited with MPA in trench, followed by PVD-Al/Reflow process and Al CMP is done with silica-based slurry. Conventional CVD-Al process is able to fill on any types of under layer in trench above 100nm design rule, but in order to achieve a complete filling for under 100nm process, a selective growth property of CVD-Al deposition, so called 'bottom up growth' is used that CVD-Al grows preferentially upward on the bottom in trench without growing of CVD-Al on top of trench. This effectively happens under 100nm trench with metal rich TiN and TiCl4 based CVD TiN stacked films. We observed a superior Al filling capability in trench with a width of 40nm by the 'bottom up growth of CVD-Al'. This shows Al interconnect by damascene process could be expandable even beyond 40nm if under-layer thickness is further optimized. In electrical property, line resistance of Al damascene is quarter of W damascene, and we study the reliability test of Al damascene process for practical application. From this work we expect that Al damascene process by 'bottom up growth of CVD-Al'could be a promising technology for fine pitch interconnect.

B8.24

A Study of Copper Electroplating in the Submicron Scale Patterns. Ui-hyoung Lee, Hyo-Jong Lee and Tak Kang; Material Science and Engineering, Seoul National University, Seoul, South Korea.

Copper electroplating process has many advantages of gap-fill performance, low cost and easy process. Therefore most manufacturers have accepted the electroplating process as one of their copper metallization processes. The most important thing of these benefits of the electroplating is the superfilling performance, which is controlled by three organic additives, accelerator, suppressor and leveler. In spite of these wide applications, its superfilling mechanism has not been studied enough for the submicron scale patterns. In this paper, additive diffusions and the concentration overpotential effect in the submicron scale pattern are discussed and the limitation of copper ion supply in the commercially used high acidic copper sulfate bath will be presented for the understanding of superfilling mechanisms. For these experiments we design 1-D pattern for one directional growth from the bottom of trench during electroplating. It has similar pattern shapes and sizes as the conventional damascene pattern which makes the three directional growths during the electroplating. This pattern generally can be shown in LIGA(lithographie, galvanik, abformung; lithography, electroforming and molding) method MEMS(micro electro-mechanical system) structures; TEOS 300nm/TaN 25nm/Cu 120nm/SiN 100nm/PR 470nm are sequentially deposited on Si substrate, and then the photo-lithography and SiN etch area processed. The SiN interlayer is essential to enhance the adhesion between copper and PR. From the experimental results for the invented pattern which has seed layer only in the pattern bottom, no superfilling is found at 200nm pattern during electroplating in case of no shrinkage of the surface area. For that reason, it means that superfilling in the damascene pattern results from the accelerator accumulation. Additionally the copper plating rates for invented patterns and various width and space patterns are almost same, and it means that concentration overpotential effect for copper electroplating in submicron scale may be negligible. Hence, it seems that copper damascene electroplating for ULSI can be regarded as the simple electroplating system controlled by the activation overpotential of organic additives' sticking, not the concentration overpotential of copper ion. By these experimental results, there is no difference of copper plating rates between wide pattern and narrow pattern at 18A/dm2 which is equal to 4000nm/min as the plating rate. It can be inferred that the copper electroplating process is applicable to the gap-filling for 100nm width pattern.

B8.25

Modeling the Impact of Packaging Stress on Device Performance. Xiaopeng Xu and Victor Moroz; TCAD R&D, Synopsys, Inc., Mountain View, California.

Current silicon technology utilizes mechanical stress engineering to tailor the bandgap and carrier mobility. The device performance can be significantly improved by the appropriately applied channel stresses. The intentional stresses are introduced into the device channel by means of epitaxial SiGe, cap layer, metal gate, STI, etc, during transistor fabrication process. To fully benefit from channel stress engineering, it is very important to maintain the intentional stresses in the channel. However, unintentional stresses are also generated during the transistor fabrication and packaging process steps. While unintentional stresses from fabrication steps such as deposition, etching, thermal ramp, oxidation, and silicidation have received most attention since they are often coupled with the intentional stresses, the impact of residual stresses on device performance from later packaging steps have not been considered in the previous studies. In this study, the impact of various types of residual stresses from chip packaging steps on device electrical performance is investigated using our process and device simulators. The residual packaging stresses are simulated by considering the thermal and material mismatch of the silicon chip, solder bumps, underfills, fillets, and the BT substrate. The residual stresses are then treated as external traction forces acting on individual transistors. The final simulated channel stresses are the results from multiple contributions including intentional and unintentional sources. Electrical properties of the transistors such as the bandgap, junction leakage, and carrier mobility, are then studied under the altered channel stresses. The numerical study shows that the residual packaging stress can be detrimental to the transistors depending on the stress pattern, the magnitude and the transistor type. Parametric studies are also carried out to examine the effects of intrinsic stress, process thermal budgets, viscous flow and material selection. The implications of the packaging stress on reliability issues such as voiding and debonding are also discussed. While experimental tracing of stresses during fabrication and packaging steps remains extremely difficult, this study illustrates that numerical modeling provides a valuable alternative.

B8.26

Material Reliability and Integration Issues of Benzocyclobutene (BCB) Interlayer Dielectric (ILD) Material. Parshuram Bakrishna Zantye[1,2] and Ashok Kumar[1,2]; [1]Department of Mechanical Engineering, University of South Florida, Tampa, Florida; [2]Nanomaterials and Nanomanufacturing Research Center, University of South Florida, Tampa, Florida.

Copper is being increasingly implemented as the interconnect wiring material and novel polymeric low dielectric constant (low- k) materials are being extensively used as ILD to decrease the Resistance-Capacitance (RC) delay in integrated circuits (IC). Multilevel metallization (MLM) scheme of interconnect wiring is fabricated to decrease the Cu wiring length. Chemical Mechanical Polishing (CMP) is the process of choice for planarization of the constituent layers of the damascene structures that make up the MLM scheme. Understanding the structural, mechanical, interfacial and tribological properties of these dielectric layers that are subjected to the CMP process is critical for successful evaluation and implementation of these materials with the copper metallization. In this research, we have studied the effect of curing temperature on material reliability and integration issues of the BCB (polymeric) dielectric material. The chemical composition and mechanical properties of BCB are studied using Fourier Transform Infra Red (FTIR) spectroscopy and nanoindentation respectively. The interfacial

and tribological properties are investigated using nanoscratch testing and polishing on the CETR CMP bench top tribometer. The temperature of curing affects the chemical properties and the bond structure as well as the cross linking of the polymeric BCB. This in turn affects the mechanical, interfacial and tribological properties of the material. The performance of the BCB dielectric material with different curing temperature has been compared with fully cured polyimide which is also a candidate dielectric material. The results of these investigations need to be taken in to account before development of a CMP process for dielectric planarization.

B8.27

Porosity Content Dependence of TDDB Lifetime and Flat-Band Voltage Shift by Cu Diffusion in Porous Spin-on Low-k. Sang-Soo Hwang[1], Hee-Chan Lee[1], Hyun Wook Ro[2], Do Yeung Yoon[2], Young-Bae Park[3] and Young-Chang Joo[1]; [1]School of Materials Science & Engineering, Seoul National University, Seoul, South Korea; [2]School of Chemistry, Seoul National University, Seoul, South Korea; [3]School of Material Science & Engineering, Andong National University, Andongsi, South Korea.

Low-k dielectric materials have been widely used in advanced metallization to reduce RC delay. In order to further decrease the dielectric constant (k), porosity is introduced into low-k materials. In general, the poor the mechanical properties as well as the electrical reliability are expected with the higher porosity. Ogawa et al. [1] studied the effect of porosity in low-k materials on Cu diffusion through the dielectric. Low-k materials with higher porosity had lower E_{bd} (breakdown voltage), β (Weibull slope), and $t_{63.2}$ (the characteristic parameter of Weibull plot); however, they used different low-k materials having different values of porosity, which lacks understanding on the porosity dependence of the same low-k material. In this paper, time-dependent dielectric breakdown (TDDB) and capacitance-voltage (C-V) tests were performed to evaluate porosity dependence of Cu diffusion in porous spin-on low-k materials. The low-k materials used in this study were consisted of the same matrix with different porogen contents. $t_{63.2}$ and β was acquired from TDDB tests, while flat-band voltage (V_{FB}) shift was obtained from C-V measurements before and after the bias-temperature stressing (BTS). The activation energy of Cu diffusion in the spin-on low-k dielectric without pore was calculated as well. The time to dielectric breakdown ($t_{63.2}$) of the spin-on low-k dielectric decreased as the porosity was increased. We observed not only an abrupt decrease in the time to dielectric breakdown but also a significant increase in V_{FB} shift when the porosity was increased from 20% to 30%. Our observation was consistent with others' [2], in which they used the positron annihilation lifetime spectroscopy (PALS) to find that the intensity of positronium escaping into vacuum increased abruptly with the porosity higher than 20%. All of these results provide a strong piece of evidence that the cross-linking of the pores begins to occur when the porosity is higher than 20%. The cross-linking of pores may result in either of change in the dominant path of Cu diffusion, i.e. from bulk to surface, or instability of the electric and mechanical properties of the dielectric with incorporation of ambient gas. [1] E. T. Ogawa et. al., Proceedings of IRPS, 166 (2003) [2] Do Y. Yoon et. al. Mat. Res. Soc. Symp. Proc. 766, pp. 241-251 (2003)

B8.28

Structure and Interfacial Reliability of Low Dielectric Constant Organosilicate Glass (OSG) Thin Films. Youbo Lin and Joost Vlassak; DEAS, Harvard University, Cambridge, Massachusetts.

As one of the leading candidates for inter-layer dielectric (ILD) materials in the next generation of integrated circuits, OSG films fabricated by plasma enhanced chemical vapor deposition (PECVD) are by far superior to other polymer-based and spun-on low-k materials due to better mechanical properties and compatibility with current fabrication process. OSG is obtained through incorporation of organic groups, such as methyl and methylene groups, into silicon dioxide matrices. The organic groups reduce the dielectric constant, but also degrade the mechanical properties of the material compared to that of silicon dioxide. The low fracture toughness and poor adhesion to barrier layer, in particular, make the material difficult to integrate and may result in cracking and delamination during processing. It is important to understand the effect of the organic groups on the bonding structure, hence the mechanical behavior of the material. Structure of OSG films of different carbon content is analyzed using Fourier Transform Infrared Spectroscopy (FTIR). Compositional information is derived from Rutherford Backscattering Spectroscopy (RBS) and Forward Recoil Elastic Spectroscopy (FRES). The interfacial reliability of OSG/barrier system is evaluated using a four-point bend testing system in ambience of different relative humidity and in aqueous conditions of various pH values. The results are rationalized in light of a structure-correlated kinetic model.

B8.29

Analysis of the Interfacial Reaction between Sn-3.5Ag and Electroplating Interlayers. Sheng-Min Yang[1], Yinyu Chang[2] and Weite Wu[1]; [1]National Chung Hsing University, Taichung, Taiwan; [2]Surftech Co, Taichung, Taiwan.

At present, Pb-free process is imperative in the electronic packaging industry. Many reports focus on Pb-free solder to improve the solderability, it seems not obtain wettability as good as SnPb solder. In this study, an alloy interlayer with different content was deposited on Cu to balance wettability and diffusion barrier in the interface of joint by electroplating process. There are four types of interlayers including Cu, Sn, Ni, and SnNi alloy. The interlayer may react with Sn-3.5Ag solder during reflow process. Sn-Ni alloy plating layer is selected to improve wettability and provide diffusion barrier at the same time in soldering process. Pull off test was used to estimate the joint strength of solder joint. For interfacial microstructure examination, morphology characterization and chemical analysis of IMC can be obtained by using scanning electron microscope (SEM) and energy-dispersive x-ray analysis (EDX). The structure of IMC is identified by x-ray diffraction (XRD). Interfacial reaction changes the type and thickness of intermetallic component (IMC) between various alloy films and Sn-3.5Ag solder and affects joint adhesion. Alloy plating layer would correspond to economic benefits and improve the reliability of solder joints.

B8.30

Electromigration of Electroplated Gold Interconnects. Steve H. Kilgore[1], Craig A. Gaw[2], Haldane Henry[2], Darrell Hill[2] and Dieter K. Schroder[3]; [1]Quality Organization, Freescale Semiconductor, Tempe, Arizona; [2]Technology Solutions Organization, Freescale Semiconductor, Tempe, Arizona; [3]Dept. of Electrical Engineering, Arizona State University, Tempe, Arizona.

Electromigration tests were performed on passivated electroplated Au four terminal Kelvin line and via interface line structures using the conventional resistance monitoring technique. The stress conditions ranged from current densities from 1.5 to 2.0 MA/cm^2 with ambient temperatures from 325°C to 375°C. Temperature Coefficient of Resistance (TCR) value was measured prior to current stressing and was used to calculate the Joule heated film temperatures. The times to failure (lifetimes) for the Au interconnects were taken as a 50% $\Delta R/R_0$ change. The median failure time was plotted against the inverse film temperature to determine the activation energy value as 0.46 $\pm$ 0.02 eV. Failure analysis of void location and suggested diffusion mechanism will be discussed. *Introduction* – The study of electromigration has emerged from fundamental diffusion studies by material scientists to statistical accelerated lifetime experiments performed by semiconductor reliability engineers in order to predict interconnect lifetimes under operating conditions. Understanding the electromigration mechanism of Au films has significant importance to GaAs based electronics such as metal semiconductor field effect transistors (MESFETs) and heterojunction bipolar transistors (HBTs) for high power applications, where Au is used for interconnects. The trend in the semiconductor industry has moved towards reduced dimensions on interconnects leading to increased current densities and operating temperatures. Both of these conditions create a raised electromigration risk in integrated circuits, where increased current density and temperature degrades the metal line electromigration lifetime. The lifetime is predicted by Black's equation and it is thus extremely crucial to have accurate values for the activation energy of electromigration. Ultimately, the need to develop more reliable metal interconnects is of primary importance and is only limited by our understanding of the electromigration mechanisms. The purpose of this paper is to present recent electromigration results on the current density and temperature behavior for Au lines typical of GaAs transistors.

B8.31

The Influence of Temperature, Structure, and Dielectric Materials on Stress Induced Voiding in Cu Dual-Damascene Interconnects. Wei Shao, Zhenghao Gan, Chandrasekar Venkataramani, Subodh G. Mhaisalkar and Ahila Krishnamoorthy; School of Materials Engineering, Nanyang Technological university, Singapore, singappore, Singapore.

Stress-induced voiding in ULSI metallization has become a serious concern with the demand of a higher circuit density and smaller feature sizes. In this work, wafer and package level stress migration test of Cu dual-damascene interconnects in via-line structures was performed. Three main factors that were considered are stressing temperature, dielectric materials, and structural reservoir. The via-line structures were studied at temperatures ranging from 150?C to 250?C, with highest failure rate being detected at 200?C. In comparing stress migration data on carbon doped oxide (CDO) with undoped silica glass (USG), a difference of two orders of magnitude was detected in the rate of change of resistance. More than 50% of the

CDO samples showed open circuit failures after a 1,000 hour test, whereas the maximum resistance change in the USG samples was only 10%. Failure analysis based on FIB indicated that failures in both CDO & USG were very similar in nature with voids forming symmetrically at the bottom of the via. The effect of M1 & M2 extensions on stress induced voiding was also studied. The M2 extension (or overhang) did not show any effect on stress induced voiding. However, M1 extensions of 0, 0.06 ?m, and 0.12 ?m showed a significant change in both CDO and USG wafers. This observation may be explained based on the changes in the stress distributions in the via region and its interaction with the Ta barrier. Finite Element Analysis (FEA) indicated that the location, gradient, and concentration of hydrostatic as well as normal stresses could explain the stress induced voiding at the via bottom. Failure analysis also indicated that the integrity of the Ta barrier in the via bottom area was of significance to stress induced voiding reliability.

SESSION B9: Interconnect Reliability Issues
Chairs: Paul Besser and Young-Chang Joo
Friday Morning, April 1, 2005
Room 2004 (Moscone West)

8:30 AM *B9.1
Passivation Effect on Stress Relaxation and Mass Transport in Electroplated Cu Films. Paul S. Ho[1], Dongwen Gan[1], Rui Huang[1], Jihperng Leu[2], Jose Maiz[2] and Tracey Scherban[2]; [1]Mechanical Engineering, The University of Texas at Austin, Austin, Texas; [2]Intel Corporation, Hillsboro, Oregon.

Electromigration in Cu damascene lines is dominated by mass transport at the Cu/cap layer interface. Stress relaxation measurements were performed using a bending beam technique to investigate the effect of passivation layer on mass transport in electroplated Cu films. A kinetic model coupling grain boundary diffusion with surface and interface diffusion was developed and found to account well for the stress relaxation observed. Based on the kinetic model, grain boundary and interface diffusivities were deduced in electroplated Cu films. Passivation layers investigated included SiC, SiNx and a metal cap layer and the effect on stress relaxation rates were compared with no passivation in order to study the effect of interfacial chemistry on mass transport. A significant effect due to different interfacial layers was observed and can be correlated to electromigration lifetime and interfacial adhesion.

9:00 AM B9.2
Fundamentals of Cu/Barrier Layer Adhesion in Microelectronic Processing. Harsono Simka[1], Sadasivan Shankar[1], Carolyn Duran[2] and Michael Haverty[1]; [1]Technology CAD - Logic Technology Development, Intel Corp., Santa Clara, California; [2]Polymer Memory Group, Intel Corp., Hillsboro, Oregon.

Copper is most widely used interconnect material in present silicon microelectronic technologies. As such, multiple interfaces formed by a thin Cu layer and other materials have to be engineered to achieve the desired chemical, mechanical, and electrical properties. Adhesion between Cu and the barrier layer, as well as between Cu and the dielectric, is of particular interest, due to its role in controlling interfacial stability and Cu electromigration behavior (1). This work focuses on understanding how the chemistry of interfaces affects adhesion. First-principles density functional theory (DFT) calculations were used to determine chemical adhesion energies of interfaces formed by Cu and various metals considered as a diffusion barrier, including Ta, TiN, and W. Calculations predicted increasing adhesion strength in the order of TiN < Si-doped TiN < TaN < Ta, consistent with wetting experiments done using 100$\AA$ thick Cu layer samples. Effects of doping of the interface using light elements (C, N, O) were determined. Calculations were also done for interfaces of Cu with two different classes of amorphous dielectric materials, i.e. silicon nitride and silicon carbide, for which detailed material characterizations are often difficult and time consuming. Quantum calculations predicted Cu/Si-nitride and Cu/Si-carbide adhesion strengths consistent with 4-pt-bend experiments, including the improvement in adhesion energies when Al or Si was used to dope the interface. These dopant effects could be explained in terms of local lattice mismatch between Cu and the dielectric layer in the interface. In addition, weaker interfaces provide low resistance diffusion paths for Cu atoms during electromigration. The first-principles based modeling, validated by select adhesion measurements, provides an effective and predictive approach to determine adhesion strengths and predict electromigration reliability in interconnects. Reference: 1. M.W. Lane, E.G. Liniger, and J.R. Lloyd, J. Appl. Phys., 93, 2003, p. 1417-1421

9:15 AM B9.3
Effect of Current Direction on the Reliability of Different Capped Cu Interconnects. Chee Lip Gan[1], Chin Yang Lee[1], Cheng Kuo Cheng[2] and Jeffrey Gambino[3]; [1]School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; [2]Institute of Microelectronics, Singapore, Singapore; [3]IBM Microelectronics, Essex Junction, Vermont.

It is widely acknowledged that the reliability of Cu-based interconnects can be improved significantly by replacing the present SiN cap layer with a different material which will slow down Cu electromigration along this interface. However, besides improving the lifetime of the interconnect, a better cap layer will also affect the dependence of lifetime on the direction of current flow. In this report, the reliability of Cu M1-V1-M2-V2-M3 interconnects with SiN and CoWP cap layers was investigated. As expected, the reliability of CoWP capped structures is much better than identical SiN capped structures. However, it was also found that the reliability of CoWP capped interconnects was independent of the direction of electrical current flow. This phenomenon was not observed for SiN capped structures, where electron current flow from "via-below" structures have about 3 times larger median-time-to-failure than identical lines with current flow from "via-above". This is because the Cu/SiN interface is the void nucleation site and the fastest diffusion pathway in such architecture. Failure analysis has shown that fatal voids consistently formed directly below the via for "via-above" configuration, and in the lines above the vias for "via-below" configuration. On the other hand, failure analysis for CoWP coated structures show that voids do not necessary form below the vias for "via-above" testing direction. This is because the adhesion of the Cu/CoWP interface may be just as good, if not better, than the Cu/Ta liner interface. As a result, voids do not nucleate at the Cu/CoWP interface and thus no small partial spanning void may form directly below the via in "via-above" configuration. In both testing directions, a large full spanning void is required to cause a failure, and thus an interconnect lifetime is independent of whether the current is flowing from "via-above" or "via-below". This phenomenon is important and its effects must be incorporated into circuit-level reliability analyses for advanced Cu-based interconnects with improved capping layers.

9:30 AM B9.4
Multi-Via Electromigration Test Structures for Identification and Characterization of Different Failure Mechanisms. Zung-Sun Choi[1], Choon Wai Chang[2], Jung Hoon Lee[3], Chee Lip Gan[4,2], Carl V. Thompson[1,2], Kin Leong Pey[4,2] and Wee Kiong Choi[5,2]; [1]Materials Science and Engineering, MIT, Cambridge, Massachusetts; [2]Materials Science and Engineering, Singapore-MIT Alliance, Singapore, Singapore; [3]Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts; [4]Materials Science and Engineering, Nanyang Technology University, Singapore, Singapore; [5]Materials Science and Engineering, National University of Singapore, Singapore, Singapore.

Experiments on dotted-I structures (copper metal lines with vias at both ends and an additional via at the center) showed that the mortality of a single segment not only depends on the values of its current density and length, but also on the stress conditions in the linked segment. The current density in one 25 micrometer (um) long segment was fixed at 0.5MA/cm$\hat{2}$, with electron flow toward the central via. In the other segment, the current magnitude and sign were varied for different test populations, with the current varied from 2.5MA/cm$\hat{2}$ to -2.5MA/cm$\hat{2}$ with intermediate values including zero. For all cases, some test structures survived for the full 780 hours of testing and some did not. The percent of the lines that failed increased monotonically with an effective jL product defined as the maximum of the sum of the jL products from all paths through the structure. However, some lines with very small effective jL products still failed, and some lines with relatively large effective jL products did not. Simulations of electromigration and electromigration-induced failures for all test conditions have been carried out. We find that test conditions leading to extreme values of the effective jL product probe different failure mechanisms than those associated with intermediate effective jL products. Multi-via test structures in general, and dotted-I test structures specifically, are shown to be versatile tools for identification and characterization of different failure mechanisms and length effects through the use of different test conditions with a single fixed structure.

9:45 AM B9.5
Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects. Robert Keller[1], Roy Geiss[1], Yi-wen Cheng[2] and David Read[1]; [1]Materials Reliability Division, NIST, Boulder, Colorado; [2]Protiro, Inc., Denver, Colorado.

We demonstrate the evolution of microstructure and deformation associated with the use of electrical methods for evaluating the thermomechanical reliability of patterned interconnects on rigid substrates. Thermomechanical fatigue in aluminum and copper interconnects was induced by means of low-frequency (100 Hz),

high-density (> 10 MA/cm^2) alternating currents, which caused cyclic Joule heating and associated thermal-expansion strains between the metal lines and oxidized silicon substrate. Such conditions can cause a cyclic temperature amplitude of approximately 100 K and corresponding cyclic stress amplitude of approximately 200 MPa. The failure mechanism differs from that observed in direct current electromigration studies due to the short cycle time, and involves formation of localized plasticity, which causes topography changes on the less-constrained surfaces of the interconnect. Open circuit eventually takes place by melting at a region of severely reduced cross-sectional area. Both aluminum and copper responded to the power cycling by deforming in a manner that was highly dependent upon variations in grain size and orientation. Isolated patches of damage appeared early within the confines of individual grains or clusters of grains, as determined by a *quasiin − situ* automated electron backscatter diffraction measurement. With increased cycling or with increased current density, the extent of damage became more severe and widespread. We document some examples of the types of damage that mechanically confined interconnects can exhibit when subjected to only thousands of thermal cycles, including growth and re-orientation of grains in a systematic, crystallographic manner. We observed that certain grains can increase by nearly an order of magnitude in size, and re-orient by greater than 30 degrees during the process. Implications of these aspects of constrained deformation on device reliability will be discussed, as will the suitability of electrical methods for accelerated testing of mechanical reliability.

10:30 AM *B9.6
The Effect of Inter-Level Dielectric and Cap on the Electromigration Reliabiliity of CU Interconnects.
Christine Hau-Riege[1], Amit Marathe[1] and Stefan Hau-Riege[2]; [1]Technology and Reliability Development, AMD, Sunnyvale, California; [2]Physics and Advanced Technologies, LLNL, Livermore, California.

We have explored the effect of the inter-level dielectric (ILD) and Cu-cap materials on electromigration reliability of Cu-based interconnects through experiment and modeling based on 130 and 90nm technologies. We have determined the mechanical properties of the surrounding ILD and Cu-cap to play a key role on the critical stress change to void nucleation (delta_sigma_crit), which is one of the critical parameters in determining electromigration lifetime or any other void-limited lifetime. Specifically, we found that delta_sigma_crit decreases as the Young's Modulus of the inter-level dielectric decreases. This finding implies that a lower build-up of stress is needed in order to nucleate a void for those interconnects imbedded in softer materials for a given Cu/cap interface energy, which in turn poses an inherent limitation on the reliability of low-k systems. The importance of the quality of the Cu/cap interface, which is currently the site of void nucleation, is therefore emphasized, where a high adhesion energy is desirable for a high critical stress change to void nucleation. Therefore, optimizations in the top Cu interface (e.g., different cap material, pre-treatment, etc.) become even more important in Cu/low-k systems in order to meet the ever-increasing electromigration reliability requirements of modern IC products. Finally, this work also provides a methodology based on modeling and experiments from which delta_sigma_crit, and therefore jL_crit, can be extracted over any range of ILD and Cu-cap properties.

11:00 AM B9.7
Characterization of Temporary Extrusion Failures in Quater-Micron Copper Interconnects.
Yan Zhang[1], Jun-ho Choy[2], Glenn H. Chapman[1] and Karen L. Kavanagh[2]; [1]Engineering School, Simon Fraser University, Burnaby, British Columbia, Canada; [2]Physics, Simon Fraser University, Burnaby, British Columbia, Canada.

We report an unusual circuit failure mode induced by short-lived extrusions observed during electromigration tests of quarter-micron damascene copper (Cu) interconnects. We employed a serpentine, via-free Cu line as the test structure, combined with isolated monitor lines, with a total length, 1800 μm. The accelerated electromigration tests were carried out at temperatures of 300 °C or 350 °C, and at a stress current density ranging from 5 to 9 MA/cm^2. A grounded external resistor of either 47 ohm or 19,980 ohm was connected to the monitor line, simulating the neighboring circuit with either low or high resistance, respectively. The leakage current between the test line and monitor lines and the resistance of the test line were recorded every 15 seconds to obtain the variation as a function of time. Our electromigration test results support the conclusion that the diffusion along the interface between the capping dielectric layer and copper metal lines is the major atomic transport path, and that extrusions form along this interface, causing short circuit failure in agreement with previous reports. Our investigations, however, also reveal that many extrusions between test and monitoring lines are temporary, self-healing after a short-lived short circuit failure. These multiple "soft failures" occur prior to the traditional permanent or "hard" failure. The time-dependent leakage current shows that the kinetics of the self-healing process accelerates as the electrical stress condition across the extrusion increases. Employing finite-difference and boundary element methods, a two-dimensional numerical simulation of the diffusional shape evolution of these extrusions was performed assuming a Cu/dielectric interface is the major atomic diffusion pathway. The numerical results show that capillary forces alone can rupture a thin and narrow copper stripe in order to reduce the interfacial free energy, and that the addition of the electron wind force across the extrusion accelerates the dissolving process in agreement with our experimental observations. Our findings suggest continuous monitoring of the leakage current between the test line and neighboring circuits and a high data-sampling frequency are necessary to detect this soft failure mode. We are grateful for funding support from the BC Advanced Systems Institute.

11:15 AM B9.8
Analysis of Electromigration-Induced Void Motion and Surface Oscillation in Metallic Thin-Film Interconnects.
Jaeseol Cho, M. Rauf Gungor and Dimitrios Maroudas; Department of Chemical Engineering, University of Massachusetts, Amherst, Amherst, Massachusetts.

Electromigration-induced void dynamics in metallic thin films is a problem of major interest for fundamental understanding of driven mass transport and for addressing important interconnect reliability concerns. Recent theoretical work in this area has depicted extremely rich nonlinear dynamical phenomena induced by electromigration and emphasized the role of the anisotropic surface diffusivity and current crowding effects in void morphological evolution and film failure. In this presentation, we focus on electromigration-induced motion of morphologically stable voids and wave propagation on morphologically stable void surfaces. Our analysis emphasizes systematic parametric study of current-induced void morphological response based on self-consistent numerical simulations of morphological evolution of voids in metallic thin films; our simulations account rigorously for current crowding effects, surface curvature effects, and the strong anisotropy of adatom diffusion on void surfaces. The mass transport problem on the void surface is coupled self-consistently with the electric field distribution in the conducting film, which is computed using a novel boundary-element method. Our analysis demonstrates that as the morphological stability limit is approached, the migration speed of a stable void deviates substantially from being inversely proportional to the void size, a well-known result that is rigorously valid in an infinite conductor with isotropic materials properties. A non-linear shape function that includes both current crowding and diffusional anisotropy effects is derived and is used to rescale properly the void migration speed resulting in a universally valid relationship for the migration speed as a function of void size. Furthermore, in grains characterized by high symmetry of surface diffusional anisotropy, our analysis predicts the onset of stable time-periodic states for the void surface morphology as either the applied electric field strength, or the void size, or the strength of the diffusional anisotropy is increased over a critical value. These stable states correspond to waves propagating on surfaces of voids that migrate along the metallic film at constant speeds; for parameter values below the critical ones, void morphological evolution leads to stable steady states. The examined nonlinear void dynamics is very rich, leading to different sequences of morphological transitions and instabilities as different operating conditions are varied.

11:30 AM B9.9
The Effect of Immersion and Evaporated Sn Coating on the Electromigration Failure Mechanism and Lifetimes of Cu Dual Damascene Interconnects.
Minyu Yan[1], King Ning Tu[1], Anand Vishwanath Vairagar[2,3], Subodh Gautam Mhaisalkar[2] and Ahila Krishnamoorthy[3]; [1]Department of Materials Science and Engineering, UCLA, Los Angeles, California; [2]School of Materials Engineering, Nanyang Technological University, Singapore, Singapore; [3]Institute of Microelectronics, Singapore, Singapore.

In sub-micron dual damascene Cu interconnects, electromigration occurs mainly along the interfaces between Cu and dielectric cap layer. Many reports have shown that the interface of Cu/dielectric cap is the dominant diffusion path. In-situ electromigration experiments were carried out recently by A. V. Vairagar etal [APPL. PHYS. LETT., 85, 2502 (2004)] to investigate the electromigration failure mechanisms in the upper and lower layers in dual-damascene Cu test structures. It was found that electromigration-induced void first nucleates at locations which are far from the cathode, then moves along the Cu/dielectric cap interface in opposite direction of electron flow, and eventually causes void agglomeration at the via in the cathode end to open the interconnect. In the present study, immersion Sn or a thin layer of evaporation Sn (20 nm) was employed after CMP and before SiN deposition. All the samples, with a line-width of 0.28 um, were assessed by package level electromigration tests at 300°C under a current density of 3.6MA/cm^2. We found that these surface

treatments effectively introduce the Cu-Sn bonding to the Cu/dielectric interface and has influenced electromigration along the Cu/dielectric interfaces. Failure analysis shows that the samples with these Sn processes have a median-time-to-failure almost 1 order of magnitude larger than the standard dual damascene samples. A careful characterization utilizing FIB and SEM cross-sectional images shows that the failure mechanism has changed due to the Sn surface treatments. After electromigration-induced void nucleation, its movement is blocked by the strong Cu-Sn bonding so that its growth is localized and occurs along grain boundaries. With the increased impedance to surface diffusion, failure analysis seems to indicate that grain boundary diffusion now participates in the void movement and growth, which is proposed to be the reason for the increased lifetime.

11:45 AM B9.10
Synchrotron X-ray Micro-diffraction Analysis on Microstructure Evolution in Sn under Electromigration.
Albert TzuChia Wu[1], KingNing Tu[1], A. M. Gusak[2], J. R. Lloyd[3], N. Tamura[4] and C. R. Kao[5]; [1]Materials Science and Engineering, UCLA, Los Angeles, California; [2]Theoretical Physics, Cherkasy State University, Cherkasy, Ukraine; [3]T. J. Watson Research Center, IBM, Yorktown Heights, New York; [4]Advanced Light Source, Lawrence Berkeley National Laboratory, Berkeley, California; [5]Chemical & Materials Engineering, National Central University, Chungli, Taiwan.

White Sn (β -Sn) thin film stripe shows a voltage drop about 10% when subjected to electromigration testing. Since β-Sn has anisotropic crystal structure, it possesses different resistivity along a-, b- and c axis. The direction of the axes determines the resistance in each grain. Under electromigration, low resistance grain tends to grow in the expense of the neighboring high resistance grains. The changes of grain orientation in the Sn stripe before and after electromigration was studied by synchrotron x-ray microdiffraction ($\sim 1\mu$m in beam diameter) to achieve grain-by-grain analysis . Grain growth involves grain boundary migration and rotation of neighboring high resistance grains. A model different from normal grain growth is proposed to describe the condition and mechanism of microstructural evolution under electromigration.

SESSION B10: Advanced Packaging Challenges
Chairs: Paul Ho and Ray Pearson
Friday Afternoon, April 1, 2005
Room 2004 (Moscone West)

1:30 PM *B10.1
Flip Chip Reliability of GaAs on Si Thinfilm Substrates Using AuSn Solder Bumps. Hermann Oppermann, Matthias Hutter, Gunter Engelmann and Herbert Reichl; Fraunhofer IZM, Berlin, Germany.

Au/Sn solder bumps are mainly used for flip chip assembly of compound semiconductors in optoelectronic and RF applications. They allow a fluxless assembly which is required to avoid contamination of optical interfaces and the metallurgy is well suited to the final gold metallization on GaAs or InP semiconductors. The discussed Au/Sn solder bumps are manufactured by electroplating gold and tin in subsequent process steps on GaAs wafers. After the deposition process the bumps consist of a thick gold layer and a thinner Sn layer on top. When the bumps are heated up above 280C a liquid solder cap forms and after solidification it consists of a gold-rich Au80Sn20 with an eutectic microstructure and a Au layer which is separated from eutectic by a layer of the intermetallic Au5Sn-phase. During flip chip assembly only the eutectic cap melts while the socket stays solid. The remaining gold acts as a compliance layer thus enhancing reliability. We will compare bumps as plated or aged with those which have been reflowed prior to assembly. The yield analysis suggest that bumps in the as plated condition or aged at elevated temperature shall be used rather than reflowed ones. The flip chip assembly using Au/Sn solder bumps of 30 to 125 micron in diameter will be presented in various optoelectronic and RF applications. An RF and reliability test vehicles comprise a GaAs chip which was flip chip soldered to a silicon substrate having impedance controlled microstrip transmission lines produced by Cu/BCB/Au thinfilm. Daisy-chain and four-point-Kelvin tests structures were designed for monitoring of the electrical contact resistance of the flip chip solder joints. Temperature cycling tests with and without underfiller were performed and the integrity of solder interconnect was electrically measured after defined cycles. Mechanical shear tests and cross-sectioning revealed the different failure modes found in underfilled and non-underfilled test samples.

2:00 PM B10.2
Effect of Electromigration on Mechanical Behavior of Solder Joints. Fei Ren[1], Jae-Woong Nah[1], Jong-ook Suh[1], Hua Gan[1], King-Ning Tu[1], Bingshou Xiong[2], Luhua Xu[2] and John H. Pang[2]; [1]Materials Science and Engineering, Univ. of California, Los Angeles, Los Angeles, California; [2]Mechanical and Production Engineering, Nanyang Technological University, Singapore, Singapore.

Polarity effect of electromigration on mechanical behavior in lead-free and composite solder joints was studied. Electromigration causes a thickness change and morphology change in intermetallic compounds (IMC) at cathode and anode. To combine electromigration and mechanical test, one dimensional metal(wire)-solder(ball)-metal(wire) structure was developed with the size of 300 um diameter. The advantage of the structure is that mechanical force and electromigration current could be applied serially or simultaneously. The current density of electromigration was 1~5*10e3 A/cm2. The working temperature was 100~150 degreeC. Tensile stress and shear stress were applied either before or after electromigration. The tensile strain rate was 3 um/min. We observed that, without electromigration, tensile stress caused a break at the middle of solders because the solder was softer. On the other hand, if combined with electromigration, the failure always occurred at the cathodes interface during tensile test. The tensile strength decreased with longer electromigration time or higher current density. In shear test, the daisy chain of solders failed alternatively at the cathodes after electromigration. The combination effect of electrical force and mechanical force on solder joint failure will be discussed.

2:15 PM B10.3
Morphology and Flux-Driven Ripening of Cu_6Sn_5 Intermetallic Compound during Solder Reaction.
Jong-ook Suh[1], Andriy Gusak[2] and King-Ning Tu[1]; [1]Materials Science and Eng., Universitiy of California, Los Angeles, Los Angeles, California; [2]Theoretical Physics, Cherkasy State University, Cherkasy, Ukraine.

In flip chip technology, spalling of intermetallic compound due to consumption of thin film under-bump-metallization (UBM) is an important reliability issue. It is known that ripening of intermetallic compound is the major mechanism of UBM consumption. However, conventional ripening theory was not able to interpret the ripening of intermetallic compound. To provide a better understanding, a new kinetic theory of a non-conservative ripening was proposed in our previous study (Phys. Rev. B66, 115403, 2002.). In present study, we compared our kinetic model with experimental data for the case of reaction between SnPb solder and Cu. First, a systematic study of intermetallic compound morphology was performed, because morphology of intermetallic compounds provides kinetic path of the ripening. We observed a transition from anisotropic to isotropic morphology of Cu_6Sn_5 intermetallic compound, according to composition of solder. When SnPb solder composition was about Sn40Pb60 to Sn60Pb40, Cu_6Sn_5 intermetallic compounds showed isotropic morphology, while partly anisotropic at other compositions. When the solder was pure tin, all the Cu6Sn5 showed anisotropic morphology. Size distribution of intermetallic compound scallops showed very good agreement with our theory. Growth rate of scallops also followed our prediction, which was $r \sim t^{1/3}$.

2:30 PM B10.4
Development of C-ring Technique for Studying Effect of Stress on Growth of Interfacial Intermetallic Compounds.
Wei Zhou, S. L. Ngoh and H. L. Pang; School of MPE, Nanyang Technological University, Singapore, Singapore.

Reliability of solder joint interconnects is a most critical issue in electronic packaging. There is the urgent need to understand reliability of lead-free solder joints because lead-free solders are replacing the conventional tin-lead solders due to legislation to ban lead usage in electronic products. In soldering process, formation of thin intermetallic compounds due to reaction between the solder and substrate is essential to achieve a good metallurgical bond. However, excessive intermetallic growth in service would lead to premature failure of the joint. Stress is known to influence growth of intermetallic compounds, but no existing method is available to study effect of stress on the intermetallic growth in a controlled manner. Therefore, we developed a novel technique to make it easy to carry out quantitative study of the stress effect at various temperatures. We machined copper substrate into an open ring in the shape of letter C, drilled two holes in the lower and upper ends of the C-ring and used a bolt to tighten the C-ring. When the C-ring is tightened, its diameter is reduced, so the tensile stress on the outer surface and compressive stress on the inner surface can be calculated quantitatively from the amount of reduction in diameter. We coated the copper C-ring with 95.5Sn-3.8Ag-0.7Cu lead-free solder, tightened the ring to apply stress to the solder-substrate interface, and used the stressed C-rings for isothermal annealing at different temperatures. We demonstrate that the specially designed specimens provide consistent and reliable results for studying effect of in-plane stress on intermetallic formation at the interfaces. It is interesting to find that compressive stress results in significantly faster interfacial intermetallic growth than tensile stress

at the same annealing temperature and applied stress level. The intermetallics at interfaces appeared either as continuous Sn-Ni-Cu or as discontinuous blocky-shaped Sn-Ni-Cu structures. Whisker-like Ag-Sn intermetallics were observed to grow from the Sn-Ni-Cu layers under compressive stress condition. The technique developed can be applied to study interfacial intermetallic growth for any types of substrates, solders or other materials (e.g., thin film coating).

2:45 PM B10.5
Micro-Impact Test on the Study of Failure Mode and Bonding Strength of BGA Balls and UBM Pad. Shengquan Ou, Yuhuan Xu and King-Ning Tu; Materials Science and Engineering, University of California, Los Angeles, Los Angeles, California.

The drop impact induced solder joint fracture has become one of the critical system failure modes of interest in the electronics industry due to the migration of market focus to portable applications. For example, cellular phones might be broken due to impact by dropping. To evaluate the joint reliability between BGA ball and under bump metallization (UBM) pad, industry widely uses shear test and pull test. Unfortunately, these tests are not satisfied to evaluate the impact reliability of solder joints, because the testing speeds are typically lower than 1 mm/s, well below the velocity of impact applied to solder joints by dropping. Some previous study by Chiu et. al. proved there is a very strong correlation between drop reliability and voiding at the UBM/solder interface. However, ball shear testing does not correlate to drop test performance, and ball pull strength is not a good indicator of shock reliability either. Therefore, how to characterize the impact reliability induced by dropping becomes very crucial. Recently, the research group from Hitachi Metals, Ltd., Japan proposed a miniature impact test for solder bumps by adopting the principle of the classic Charpy impact test. Based on their work, we have designed a micro-impact testing machine to quantitatively study the bonding strength between BGA ball and UBM pad. The sample is placed on an XYZ-adjustable positioning stage. The initial position of the hammer and its final position after impact are recorded by an angle recorder with accuracy of ± 0.5 degree. Since the measured angle difference in a typical impact test is about 10 degree, the resolution is about 5 to 10% of the measured energy change. Lead-free solder balls are used in this study with 760μm size. The UBM structure is deposited Au/Ni/Cu metallization. Scanning electron microscopy is employed to study the fractured surface of the solder joints. In the study, we observed a ductile-to-brittle transition in the solder joints, due to interfacial intermetallic compound formation caused by aging. The effect of solder composition, aging temperature and time on the ductile-to-brittle transition will be further discussed. The distribution of fracture toughness of area array of solder bumps on 3cm$\times$3cm square substrate will be reported.

3:15 PM *B10.6
A New Approach for Predicting the Onset of Disbonds in Flip-Chip Assemblies. Ray Pearson and Brian J. McAdams; Materials Sci. & Eng., Lehigh University, Bethlehem, Pennsylvania.

Reliability studies on flip-chip assemblies point to the need for a study of the initiation of interfacial disbonds. A standard method for evaluating the propensity of disbond formation does not formerly exist. Therefore, we propose the use of a stress singularity approach to this problem. Our approach uses a fracture mechanics-like parameter, the critical stress intensity factor for the stress singularity, to serve as a criterion for the onset of delamination. Testing of this kind requires no measurement of pre-existing flaws, only that the geometry has a stress singularity that induces disbonds. Commercial flip-chip packages contain a variety of stress singularities of varying strengths that can promote disbonds. For our purpose, a simple geometry utilizing a butt tensile joint is employed to examine the effect of free-edge and free-corner singularities on the initiation of disbonds. This approach is used to study disbond initiation under monotonic and cyclic loading conditions. Interestingly, a strong correlation is found between disbond initiation and disbond propagation. Moreover, the ranking of fatigue behavior correlates well with static adhesion tests. Results for both model and commercial underfill resins will be presented.

3:45 PM B10.7
Low Temperature Ultra-Thin Titanium-Based Wafer Bonding. Jian Yu[1], Yinmin Wang[2], Hassa Bakhru[3], Jian-Qiang Lu[1] and Ronald J. Gutmann[1]; [1]Rensselaer Polytechnic Institute, Troy, New York; [2]Lawrence Livermore National Laboratory, Livermore, California; [3]University of Albany-SUNY, Albany, New York.

Three-dimensional (3D) wafer-scale integration is receiving increased attention with various bonding approaches, including oxide-to-oxide, dielectric adhesive and copper-to-copper. In this study, an alternative metal-based wafer bonding using an ultra-thin titanium (Ti) coating was explored. An oxidized silicon wafer was successfully bonded with a prime silicon wafer at low temperature (400°C) with 30 nm sputtered Ti as adhesive. The bonded pairs evaluated with scanning acoustic microscopy (SAM) and a series of mechanical integrity tests indicate uniform bonding over 200 mm diameter wafers with sufficient bond strength to survive downstream back-side thinning processes. The interfacial morphologies were examined by high-resolution transmission electron microscopy (HRTEM), while the chemical compositions at the intermediate region were analyzed with energy dispersive X-ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS) elemental mapping. Rutherford backscattering spectrometry (RBS) and X-ray photoelectron spectroscopy (XPS) were also applied to understand the bonding mechanisms. The results suggest that diffusion assisted solid phase reaction is responsible for the strong bonding achieved at low temperatures. Besides, the unique ability to reduce native silicon dioxide (SiO2)even at much lower temperatures makes Ti an excellent adhesion promoter.

4:00 PM B10.8
Effects of Bonding Process Parameters on Wafer-to-Wafer Alignment Accuracy in Benzocyclobutene (BCB) Dielectric Wafer Bonding. Frank Niklaus[1], R. J. Kumar[1], J. J. McMahon[1], J. Yu[1], T. Matthias[2], M. Wimplinger[3], P. Lindner[3], J. -Q. Lu[1], T. S. Cale[1] and R. J. Gutmann[1]; [1]Focus Center - New York, Rensselaer: Interconnections for Hyperintegration, Rensselaer Polytechnic Institute, Troy, New York; [2]EVGroup, Schaerding, Austria; [3]EVGroup Inc., Tempe, Arizona.

Wafer-level three-dimensional (3D) integration is an emerging technology to increase the performance and functionality of integrated circuits (ICs). Aligned wafer-to-wafer bonding with dielectric polymer layers (e.g., Benzocyclobutene (BCB)) is a promising approach for manufacturing of 3D ICs, with minimum bonding impact on the wafer-to-wafer alignment accuracy essential. In this paper we investigate the effects of thermal and mechanical bonding parameters on the achievable post-bonding wafer-to-wafer alignment accuracy for polymer wafer bonding with 200 mm diameter wafers. The initial attainable wafer-to-wafer alignment accuracy with commercial equipment is on the order of one micron prior to bonding. During wafer bonding, the wafers can shift relative to each other by several microns if the wafer bonding process parameters are not adequately controlled. Two major factors affecting wafer-to-wafer alignment on the order of several microns have been identified: (1) differences in thermal expansion of the wafers due to temperature differentials between wafers during bonding; and (2) inhomogeneities in BCB reflow process during the bonding/curing process under compression and/or slight shear forces at the bonding interface resulting from wafer warpage and/or wafer thickness variations. Our baseline wafer bonding process with uncured BCB has been modified to use partially (50-60%) cross-linked BCB. In addition, bonding conditions, including process profiles of bonding pressure and temperature ramping, have been modified. The partially cured BCB layer does not reflow during bonding, minimizing the impact of inhomogeneities in BCB reflow under compression and/or slight shear forces at the bonding interface. As a result, minimum wafer-to-wafer alignment shift ($\sim$1 micron) has been achieved and significantly improved post-bonding alignment yield obtained in initial qualification tests. Analysis of the wafer bonding process impact on post-bonding wafer-to-wafer alignment will be presented.

4:15 PM B10.9
Interconnects for Elastically Stretchable and Deformable Electronic Surfaces. Joyelle Elizabeth Jones, Stephanie P. Lacour and Sigurd Wagner; Electrical Engineering, Princeton University, Princeton, New Jersey.

We have discovered that metal lines on an elastomeric substrate can be stretched by up to 100% and remain electrically conducting. Therefore they can be used as interconnects for elastically deformable electronic surfaces. These are a new kind of macroelectronic circuit technology that integrates rigid subcircuit islands on elastomeric substrates. It may find application in circuits conformally shaped to the surface of a product, as electronic skin, and for biomechanical electronics. While the overall surface of the elastic circuit may be stretched reversibly by 10% or more, the subcircuit islands are designed to undergo strains of only 0.1% or less, to protect the devices from fracture. The elastomeric substrate exposed between the islands, and with it, the metal interconnects, accommodate most of the stretching deformation. At a high fill factor by subcircuit islands, the stretching deformation of the metal interconnects between the islands can become very large. Our task has been to make highly and reversibly stretchable interconnects at high pitch. Because of their susceptibility to organic solvents, elastomeric substrates must be processed very differently from silicon integrated circuits. Here we describe the steps we have taken so far to develop patterning techniques for the interconnect metal. Absent from any process technology, we started out by using shadow masks, which resulted in interconnects with a smallest width of 200 micrometers. Riston patternable dry resist brought the width down to 100 um. After

developing a modified photoresist process that does not require the use of organic solvents, we now have obtained 2-um wide conductors. We will first describe this patterning process. Then we will show the electrical, structural, and mechanical evaluation of the interconnects, relaxed, during mechanical cycling, and under large mechanical strain. This research is supported by the Packard Foundation, DARPA, and NSF

4:30 PM B10.10
High-Resolution Characterization of Buried Interfaces for Advanced Interconnect Architectures. Shriram Ramanathan[1], Patrick Morrow[1], Evan Pickett[1], Yongmei Liu[2] and Rajen Dias[2]; [1]Components Research, Intel Corp., Portland, Oregon; [2]Assembly Technology Development, Intel Corp., Chandler, Arizona.

Wafer-to-wafer or chip-to-chip stacking is one of the key enablers for three-dimensional (3-D) integrated circuits; heterogeneous integration of devices and advanced packaging applications. The advantages of this approach include performance improvements due to decrease of the interconnect delays, integration advantages from the opportunity of integrating divergent process flows, and reduced form factors arising from geometrical advantages of 3-D wafer (or chip) stacking. Wafer bonding (or die bonding) utilizing high-density interconnections between the two wafers is one the key steps in the overall process flow to fabricate such 3-D structures. Voids in bonded interfaces can create severe problems during further processing of such stacked wafers besides yield loss. In this paper, we discuss and benchmark different metrology techniques to analyze and quantify the quality of bonded interfaces. Acoustic microscopy (CSAM) is used to investigate interconnections between bonded wafers at high resolution. The imaging resolution is shown to critically depend on the wafer thickness through which the acoustic waves have to traverse to form the images. We present detailed theoretical analysis which shows the effect of lens aberrations on the image formation and the corresponding resolution degradation. We have also performed detailed thermal microscopy to characterize the bonded interfaces: voided regions can be imaged as localized hot spots. The temperature rise at the hot spot is shown to be primarily dependent on the defect depth and size. We show examples on how the thermal imaging can be used as a complementary metrology technique to acoustic microscopy to inspect the buried interfaces. Infra-red imaging, besides being used to analyze wafer-to-wafer alignment accuracy can also be used to investigate the quality of bonded interfaces. The void size can be calculated from the number of interference fringes arising due to the voids; however the metallization in the wafers can minimize the contrast due to the defect. We discuss both experimental results and theoretical studies of each of these different techniques to analyze buried interfaces and discuss their relative capabilities for inspection of advanced interconnect and packaging architectures.

4:45 PM B10.11
Scanning Near-Field Acoustic Holography (NFAH): Novel High Resolution Sub Surface Imaging for Embedded Features. Gajendra Shekhawat[2], Ethan Young[1] and Vinayak Dravid[3]; [1]Material Science and Engineering, Northwestern University, Evanston, Illinois; [2]Institute for Nanotechnology, Northwestern University, Evanston, Illinois; [3]Material Science and Engineering, Northwestern University, Evanston, Illinois.

As materials, structures and phenomena continue to shrink, and the micro/nanofabrication paradigms move from planar to 3-D/stacked platforms, there is an acute need to image and analyze surface/sub-surface features and phenomena at ultra-high resolution and sensitivity, coupled with usual ergonomic/economic considerations. Keeping view of these technological challenges and to overcome those, we have developed a turn-key Near-Field Acoustic Holography (NFAH) system. This unique system will address emerging issues in imaging and analysis of diverse embedded nano and microscale structures, and engineered systems. In NFAH, one high frequency acoustic wave is launched from below the specimen, and another one on the cantilever of the scanning probe microscopy (SPM) system, albeit at a slightly different frequency. The resultant beat frequency which forms as a pseudo-standing wave on the specimen surface, acts as a reference lattice. Any perturbation to phase and amplitude of the specimen acoustic wave is then measured with SPM tip as an antenna, and converted in a quantitative pictorial map. Thus, internal features, e.g., voids, cracks, phases, which perturb the acoustic wave, can be seen in such images. This technique will fill a critical void in characterization and investigation of the static and dynamic mechanics of nanoscale systems, ranging from engineering systems to biologically active structures, in-vitro. In the presentation, we will report efficacy of NFAH approach, starting with a model subsurface microstructure of buried Au nanoparticles/prisms underneath a polymer film. These embedded features are readily imaged with NFAH providing proof-of-concept of this novel approach. Additional results on practical systems will be presented, such as high resolution sub-surface imaging of copper vias (without doing any cross-sectioning), metal semiconductor composite structures, low-k dielectrics, and internal features of carbon nanotubes, nolecules, stress migration in MEMS devices and 3D Interconnects among others. It will be argued that ramping the acoustic frequency to 100 MHz would enable the extraction of subsurface defects (voids, delamination) with spatial resolution < 5 nm.