Dual-Gate MOSFETs on Monolayer CVD MoS_2 Films

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Monolayer MoS_2 with a direct band gap of 1.8 eV is a promising two-dimensional material with a potential to surpass graphene in next generation nanoelectronic applications.[1-3] We have synthesized monolayer MoS_2 thin films via chemical vapor deposition (CVD) method on Si/SiO_2 substrate and comprehensively study the device performance and variation on dual-gated MoS_2 field-effect transistors. Over 100 devices are studied to obtain a statistical description of device performance on monolayer CVD MoS_2. We have achieved record high drain current of 62.5 mA/mm in CVD monolayer MoS_2 films ever reported.[4] We further extract the intrinsic contact resistance of low work function metal Ti on monolayer CVD MoS_2 with an expectation value of 175 Ω·mm, which can be significantly decreased to 10 Ω·mm by appropriate gating. By taking the impact of contact resistance into account, average and max intrinsic field-effect mobility is estimated to be 13.0 and 21.6 cm^2/V·s in monolayer CVD MoS_2 films.

The MoS_2 crystal growth was carried out in a furnace on 285 nm SiO_2 capped p^{++} Si substrate by sulfurization of MoO_3 via CVD method shown in Fig. 1(a). Optical and AFM images of the monolayer MoS_2 crystals with triangle domains are shown in Fig. 1(b) and (c). MoS_2 crystals are single layers with good uniformity. [5] After material synthesis, source/drain regions are defined with e-beam lithography followed by Ti/Au deposition as contacts. After a 1 nm Al deposition as the seeding layer, 15 nm Al_2O_3 was grown at 200ºC by ALD used as top gate dielectric. Ni/Au that covers the whole channel served as the top gate. Fig. 2(a) shows the schematic device structure of the dual-gate MoS_2 MOSFET. Over 100 devices were fabricated with channel length varied between 100 nm to 1 μm. Fig. 2(b) shows the output curves of a 100 nm channel length back-gate devices with record-high maximum drain current of 62.5 mA/mm. Fig. 2(c) shows the output curves of a 1μm channel length top-gate devices showing the flexibility of the dual gate device to be modulated by either gates. Maximum drain current of this device is 2.71 mA/mm and 14.9 mA/mm for top-gate and back-gate modulation, respectively. The difference is attributed to the larger contact resistance on top-gate configuration. Average drain current at various channel length is 36.7±14.2, 27.1±12.2, 22.3±10.0 and 12.9±5.0 mA/mm for 100, 200, 500 nm and 1 μm channel lengths, as plotted with maximum values in Fig. 3, showing the scaling properties of transistors. The total resistance for top-gated device is mostly contributed by contact resistance, which is plotted in Fig. 4, with an expected value of R_c=175 Ω·mm without back-gate biasing. The large value of R_c explains the early saturation in transfer curves of top-gated device, as shown in inset of Fig. 4. The contact resistance at 100 V back-gate voltage can be extracted to be R_c=10 Ω·mm in Fig. 5 by TLM. [6,7] The intrinsic field-effect mobility is estimated from peak transconductance after subtracting the contact resistance. Average and maximum values of intrinsic field-effect mobility are plotted in Fig. 6 with the highest mobility of 21.6 cm^2/V·s.

In conclusion, we synthesized monolayer MoS_2 films by CVD method. We systematically studied the device performance based on these CVD films at various channel length. We achieved the highest drain current of 62.5 mA/mm at 100 nm channel length and maximum intrinsic mobility of 21.6 cm^2/V·s.

Reference:

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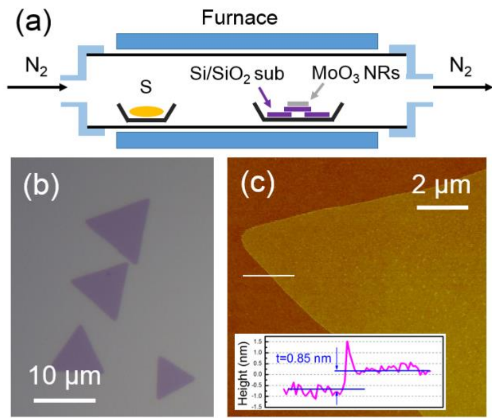

Fig 1. (a) Schematic view of CVD synthesis of monolayer MoS_2 in a tube furnace. (b) (c) Optical and AFM image of CVD MoS_2 films showing good uniformity.

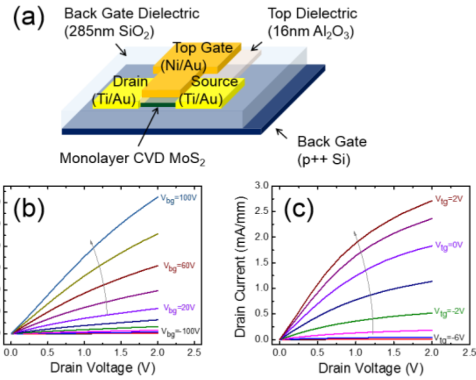

Fig. 2: (a) Schematic view of a dual-gate MoS_2 MOSFET. (b) Output curves of 100 nm L_{ch} back gate device (c) Output curves of a 1 μm L_{ch} device under top gate bias.

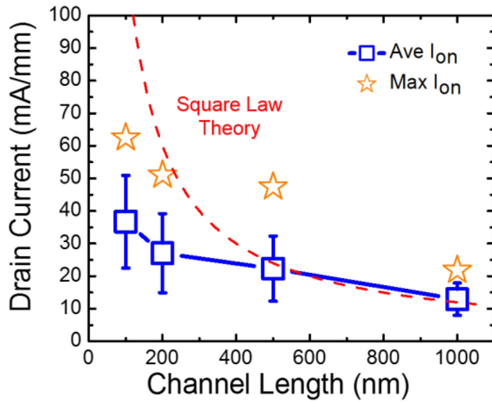

Fig 3: Averaged and maximum values of drain current at various channel lengths. Red dashed line shows Square Law Model prediction.

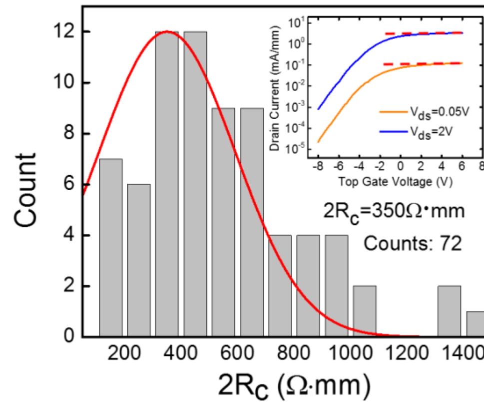

Fig. 4: Intrinsic $2R_c$ distribution in all top-gated devices with an expectation value of 350 Ω·mm. Inset: Transfer curves from a top-gate device showing early current saturation.

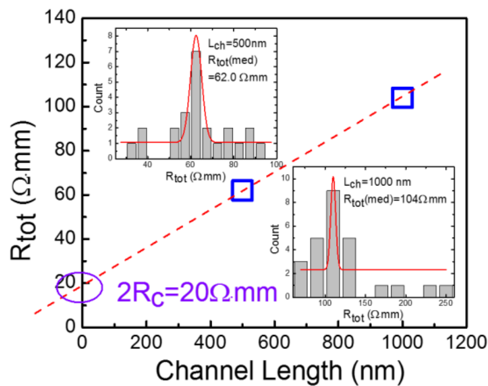

Fig. 5: Total resistance distribution in 500 nm and 1 μm L_{ch} devices at 100 V back gate bias. $2R_c$ is extracted to be 20 Ω·mm by TLM.

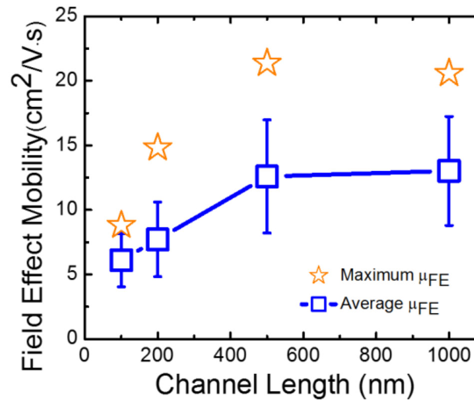

Fig. 6: Average and maximum values of intrinsic mobility with all channel lengths. We achieve the highest value to be 21.6 cm^2/Vs.